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1. INTRODUCTION TO MMS SPECIFICATIONS

This document provides the interface specifications for designers to develop any component of the Modular Measurement System (MMS). The intent of this document is to precisely define the interfaces that are important for compatibility of system components, but to leave open areas for future system growth.

The architecture concepts are based on the modular instrument architecture developed in the early 1980's. This architecture was developed to provide an environment where microwave measurement systems could be built out of modular instruments. A standardized display interface was included as an important attribute of the system, as the display of an instrument is often an important aid to test program development as well as manual operation.

Modularity in large Automatic Test Equipment (ATE) systems was recognized as an important attribute in the 1980's because of potential size reduction, serviceability improvements, and the ability to reconfigure. The United States Air Force, Navy, and Army reflected this in their requirements for ATE systems. Modular instrument solutions for digital and low frequency analog applications became possible using card-based architectures. Modular test equipment solutions for microwave applications were being built using MMS equipment.

The MMS Consortium was formed to develop the Modular Measurement System Specification so that the MMS architecture could be available to the public. This specification defines the interfaces of all MMS system components. It also allows future system enhancements with compatibility for the large installed base of MMS systems. MMS addresses the needs of microwave test systems and other applications where modularity and sensitive measurement capability are needed.

1.1 Member Representatives

Questions about this specification or the MMS Consortium may be addressed to the MMS Consortium secretary.

TABLE 1-1. Member Company Representatives

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Mario Bilac General Electric Company 1800 Volusia Avenue Daytona Beach, FL 32114	Richard Hejmanowski Microsource, Inc. 1269 Corporate Center Parkway Santa Rosa, Ca. 95407
Martin Jungman Grumman Aerospace Corporation Bethpage, NY 11714-3582	Hank Podobinski Tern Technology, Inc. 1747-22 Veterans Memorial Hwy Islandia, NY. 11722
Greg Anderson Hewlett-Packard Company 1212 Valley House Drive Rohnert Park, Ca. 94928	MMS Consortium c/o Tom Hoppin, Secretary Hewlett-Packard Company 1212 Valley House Drive Rohnert Park, Ca. 94928

1.2 Specification Objectives

This specification defines a modular instrument system architecture allowing for the compatible operation of modules and instruments. The system has been developed to meet the following objectives:

1. Define mechanical and electrical interfaces where mainframes and modules can be interchanged with full functionality in their system application.
2. Specify cooling, power, and electromagnetic compatibility requirements for mainframes and modules.
3. Specify a common digital communication bus to be used for module to module communication so that multiple conversations can occur on the bus without high-level arbitration between modules.
4. Specify the protocol needed to achieve system communications and orderly communications between modules.
5. Define a common control interface for computers external to the modular instrument system.
6. Allocate link types and register languages to insure communication compatibility between MMS devices.
7. When extending the system to incorporate new requirements, maintain backwards compatibility of the installed instrument base.

1.3 Applicable Documents

The following documents are referenced by this specification:

[1] American National Standards Institute/Institute of Electrical and Electronics Engineers, Inc. 1987. Standard Digital Interface for Programmable Instrumentation. IEEE 488.1-87 Institute of Electrical and Electronics Engineeers, Inc., Piscataway, NJ

[2] Electronic Industries Association. 1978. Electrical Characteristics of Balanced Voltage Digital Interface Circuits. EIA 422-A-78 Electronic Industries Association, Washington, D.C.

[3] Electronic Industries Association. 1983. Withstanding Voltage Test Procedure for Electrical Connectors (R 1990). EIA 364-20A-83 Electronic Industries Association, Washington, D.C.

[4] Electronic Industries Association. 1978. Insulation Resistance Test for Electrical Connectors (R 1990) EIA 364-21A-83 Electronic Industries Association, Washington, D.C.

[5] Modular Measurement System Consortium. 1992. Keyboard Graphics, and Storage Language Reference. Modular Measurement System Consortium

1.4 Terminology

1.4.1 Definition of Modular Measurement System Terms

AMBIENT TEMPERATURE -- Temperature of the air surrounding a system.

BULK AIR TEMPERATURE -- For fully developed air flow, the temperature that would result, at the module air exit in a system under test, if the air were thoroughly mixed to a uniform temperature.

CONTROL LINK -- The link provided by a logical module for control of its functions.

DATA MESSAGE -- One or more packets sent with the command bit false.

DATA STREAM -- The sequence of data sent over MSIB representing one direction of the communication over a link.

DATUM -- A theoretically exact point, axis, or plane derived from the true geometric counterpart of a specified datum feature. A datum is the origin from which the location or geometric characteristics of features of a part are established.

EXTERNAL LOOP -- The bus connecting mainframes in a multiple mainframe system.

GRAPHICS LINK -- A link which uses the registered graphics language defined in the Keyboard, Graphics, and Storage Language Reference.

INSTRUMENT -- One or more modules which together provide a function.

INTERNAL BUS -- The fifty pin bus connecting modules and the mainframe.

KEYBOARD LINK -- A link which uses the registered keyboard language defined in the Keyboard, Graphics, and Storage Language Reference.

LANGUAGE -- The ASCII sequence of characters sent over a link and used to perform actions in a module.

LINK -- The standard bi-directional communication mechanism used on MSIB.

LOGICAL MODULE -- A device which is capable of communicating over MSIB.

MAINFRAME -- The enclosure that houses Modular Measurement System modules providing the mechanical support, power, cooling, and communication bus.

MAINFRAME DATUM -- An origin from which the location or geometric characteristics of features on a mainframe are established.

MAINFRAME EXTERNAL MSIB CONNECTOR -- A thirty seven pin connector, located on the mainframe, connecting the external bus loop between mainframes.

MAINFRAME MSIB CONNECTOR -- A fifty pin connector, located on the mainframe, connecting the internal bus between modules and mainframes.

MASTER -- A module which is capable of controlling other logical modules over a control link. It is not necessary for a master to have slaves.

MMS -- Modular Measurement System.

MMS COMPONENT -- This term is reserved for only those products that fully comply with the rules of this specification.

MODULE -- A single mechanical unit that plugs into a mainframe and occupies one or more physical slots.

MODULE DATUM -- An origin from which the location or geometric characteristics of features on a module are established.

MODULE MSIB CONNECTOR -- A fifty pin connector, located on the module, connecting the internal bus between modules and mainframes.

MSIB -- The Modular System Interface Bus provides communication between logical modules. It connects logical modules over the internal bus and external loop.

MSIB STATUS MESSAGE -- The STATUS MSIB command and message

MULTIPLE MODULE INSTRUMENT -- An instrument containing more than one module.

REGISTERED LANGUAGE -- A registered language is a language which has been registered by the MMS Consortium and a link number has been assigned.

REGISTERED LINK -- A registered link is a link which has been associated with a particular language for a common MMS system function.

SLAVE -- A module which is controlled by another logical module over MSIB. A logical module, which is a master, can also be a slave.

SLOT -- The smallest single unit of a mainframe which is fully capable of mechanically and electrically supporting a module. A one slot module has historically been referred to as one eighth module.

STORAGE LINK -- A link which uses the registered storage language defined in the Keyboard, Graphics, and Storage Language Reference.

1.4.2 Compliance Terminology

The following headings are used throughout this document to clarify what is required to comply with this specification. Text which is not labeled with these headings is a description of the Modular Measurement System architecture and operation.

RULE

Compatibility of system components is achieved through the rules of the Modular Measurement System specification. It is **MANDATORY** that rules be followed to maintain compatibility. The words **MUST** and **MUST NOT** are used exclusively in the description of rules.

RECOMMENDATION

Vital information and advice to the designer is provided through recommendations. It is likely that problems will develop when recommendations are not followed. They should be followed in order to provide the most suitable system components.

SUGGESTION

Helpful information is provided through suggestions. This advice should be used to help make design decisions for Modular Measurement System system components. Suggestions are useful to designers who are not experienced in Modular Measurement System design.

PERMISSION

Clarification of otherwise unspecified areas of the specification is provided with permissions. They reassure the designer that a particular approach is within the spirit of the specification and will not be likely to cause problems at a later date. The word **MAY** is reserved for use in permissions.

OBSERVATION

The rationale behind and implications of rules is pointed out by observations. A more complete understanding of rules is developed through observations. Implications of Modular Measurement

System rules that might be overlooked are explained through observations.

1.4.3 State Diagram Notation

State diagrams throughout this specification are represented with the following notation. Figure 1-1 is an example of the notation used to represent a state diagram.

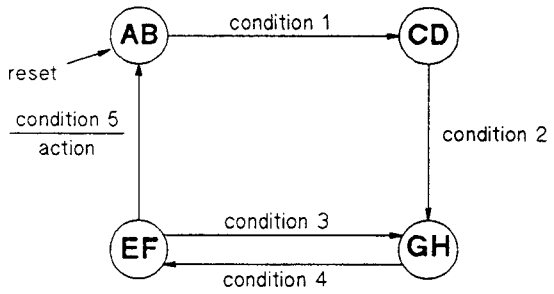


Figure 1-1. Example of a State Diagram

A state is represented by a circle. An upper case mnemonic is used within the circle to identify the state. Transitions between states are indicated by arrows. Only the indicated transitions are allowed.

The condition associated with each arrow evaluates to a Boolean value of TRUE or FALSE. If, and only if, a condition evaluates to TRUE will the function transition to the state pointed to by the arrow. When a condition evaluates TRUE the current state is left immediately and the function does not respond to any other transition conditions from the current state. The next state may be entered at any time after the condition evaluates to TRUE.

A condition is constructed from one or more local messages and/or remote messages combined using the operators AND, OR, or NOT. Local messages are generated on the internal side of the interface. Remote messages are generated on the external side of the interface. Local messages are represented by a mnemonic written in lower case. Remote messages are represented by a mnemonic written in upper case. The AND operator is represented by the symbol &. The OR operator is represented by the symbol |. The AND operator takes precedence over the OR operator unless otherwise indicated with parenthesis. The NOT operator is indicated by a horizontal bar placed above the items to be negated.

An action associated with a transition may be represented with a line underneath the condition and a mnemonic representing the action placed below the line. Condition 5 in figure 1-1 illustrates the use of an action associated with a condition.

A shorthand notation is used to represent a transition to a state from all other states of the diagram. An arrow with a condition at its origin is used to represent this condition, and is assumed to originate in all states.

1.4.4 Over Bar Notation

A bar drawn above a signal mnemonic indicates: action initiated on signal high to low transition for an edge significant signal or low on a level significant signal.

1.5 Number Representations

All numbers are given in decimal form unless followed with a suffix of "H" which is used to indicate a hexadecimal number.

When there is a fixed string of digits with some variable digits, the variable digits are indicated with an "x".

For binary data, bit 0 is the least significant bit.

1.6 Modular Measurement System Architecture Overview

The Modular Measurement System architecture is based on standard sized modules, in increments of a minimum module width, with external support functions provided by the mainframe. The mainframe provides modules with power, cooling, physical structure, and digital communication capabilities.

Two methods of digital communication are provided by the Modular Measurement System architecture. A common IEEE-488.1 interface is provided to each module interface connector, providing a standardized computer-to-instrument interface. The Modular System Interface Bus (MSIB), provides general purpose high speed digital communication between logical modules and also provides a standardized computer interface. The MSIB system also defines an extension between mainframes, allowing module placement to be dependent only upon instrument and measurement system requirements.

There are, at the time of printing, three registered languages defined by the Modular Measurement System:

- **graphics language** - allows an instrument to display text and graphics.
- **keyboard language** - allows the user to provide input to the instruments in the system.
- **storage language** - allows an instrument to access secondary media via a storage link.

An example of an MMS system is shown in figure 1-2. The block diagram corresponding to this system is given in figure 1-3. There are seven instruments in this system, made up of twelve modules. These instruments are controlled by an external computer over IEEE 488.1. One of the mainframes contains a module which supports graphics and keyboard links which can be used for monitoring any of the instruments during test program development or for manual operation. The modules can communicate using MSIB. Note that the MSIB is also connected between mainframes with the external MSIB cables.

A computer can also use MSIB to control MMS instruments. Outside of a mainframe the computer could have an external MSIB interface used to communicate with modules in the system. A computer in a module would provide the benefits of the MMS form factor and could utilize MSIB for instrument control.

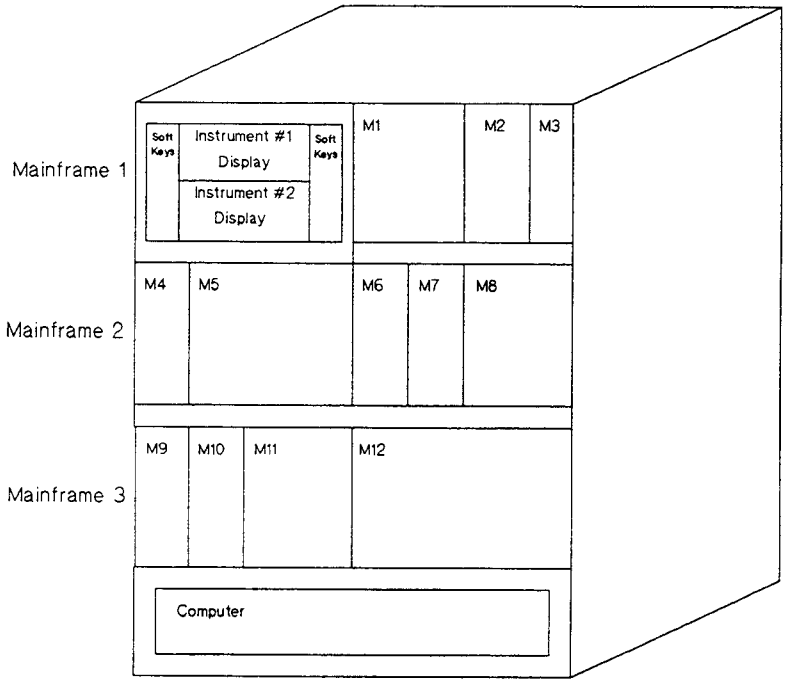


Figure 1-2. Example MMS System

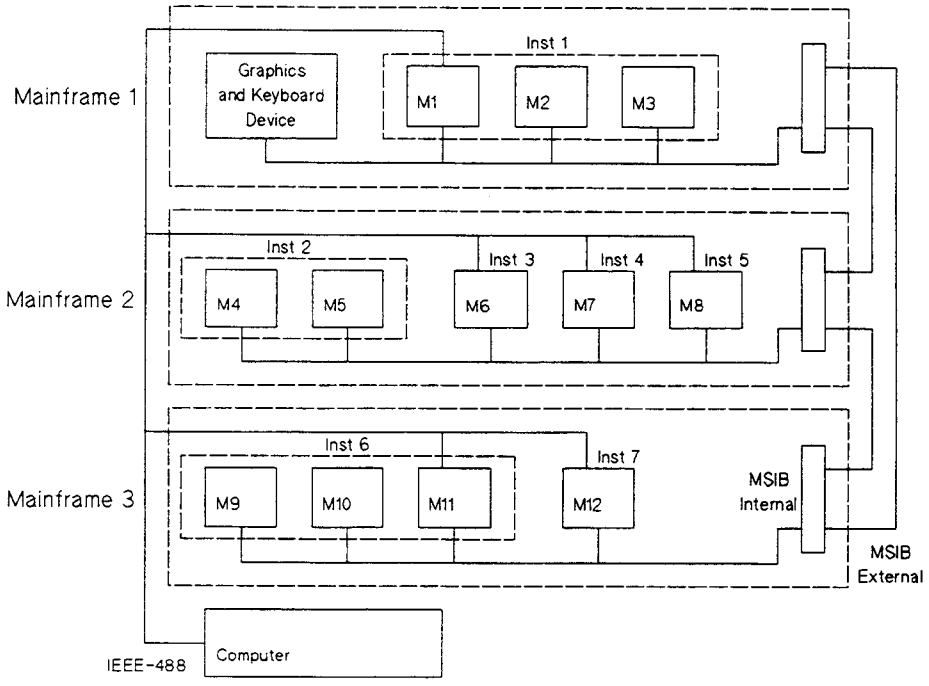


Figure 1-3. Example Block Diagram

2. IEEE STD. 488.1 INTERFACE BUS

A complete electrically equivalent set of IEEE Std. 488.1 interface lines are provided to each module MSIB connector. This includes the eight data lines (DIO1-DIO8), the handshake lines (NDAC, NRFD, DAV), the general bus management lines (EOI, REN, SRQ, ATN, IFC), and five ground return lines.

2.1 Mainframe IEEE Std. 488.1 Requirements

RULE 2.1-1:

A Modular Measurement System mainframe **MUST** provide the complete set of IEEE Std. 488.1 lines specified by the mainframe MSIB connector.

OBSERVATION 2.1-2:

The mainframe IEEE Std. 488.1 signal lines should be considered as an extension of the IEEE Std. 488.1 cable.

2.2 Module IEEE Std. 488.1 Requirements

RULE 2.2-1:

The module MSIB connector pins designated for IEEE Std. 488.1 signal functions **MUST NOT** be used for any purpose other than designated by IEEE Std. 488.1.

RECOMMENDATION 2.2-2:

Instruments should implement an IEEE Std. 488.1 interface to serve as a remote interface to a computer. The user of a Modular Measurement System expects that Modular Measurement System instruments are controllable using IEEE Std. 488.1.

RECOMMENDATION 2.2-3:

A multi-module instrument should not use IEEE Std. 488.1 to communicate between logical modules. Since the IEEE Std. 488.1 interface is the primary interface between an external computer and Modular Measurement System instruments, module to module communications would interfere with one of the primary missions of the Modular Measurement System.

OBSERVATION 2.2-4:

The IEEE Std. 488.1 interface is not the only remote control interface in the Modular Measurement System. An MSIB interface is also recommended for all modules (see recommendation 4-1).

RULE 2.2-5:

If a logical module with an IEEE Std. 488.1 interface also has an MSIB interface it **MUST** have a means to logically disconnect its IEEE Std. 488.1 interface.

RECOMMENDATION 2.2-6:

If a logical module with an IEEE Std. 488.1 interface is likely to be configured so the IEEE Std. 488.1 interface is not used, a means should be provided to electrically disconnect the interface to reduce loading on the IEEE Std. 488.1 bus.

3. POWER BUS

The MMS power system distributes 40 kHz AC waveform power to the MMS modules. Each module has a small 40 kHz isolation transformer at its input to reduce power related ground currents. This system reduces EMI and allows accurate sub microvolt sensitivity measurements. This approach also allows each module the flexibility to define its own power supply voltages without adding complexity to the mainframe.

MMS module DC power supplies use LC input filters with continuous inductor current. The output of these filters is proportional to the AVERAGE (not RMS) of the input voltage, so it is necessary that the mainframe power supply regulate the AVERAGE AC output voltage in order to minimize variations in module DC voltages.

The power system also distributes a Line Sync signal to each module. This signal is used by modules which wish to synchronize measurements to the AC line frequency.

Power and Line Sync are delivered to the modules through the mainframe MSIB connectors. Refer to appendix A, *Connector Pin Descriptions,* for further information related to the MSIB connector.

3.1 Mainframe Power Bus Specifications

RULE 3.1-1:

A mainframe **MUST** supply 40 kHz power with the specifications shown in table 3-1 when presented with any legal module load. The suggested test procedure for mainframe dynamic voltage accuracy is described in section B.1.2.2.

TABLE 3-1. 40 kHz Power Bus Specifications

Voltage:	40 kHz AC, maximum ± 20 volts peak on each phase to ground, 24.3 average line to line, +1%, -2% static, ± 1% dynamic, differentially balanced with an ohmic DC connection to ground of less than 100 mΩ.
Frequency:	40 kHz ±5%.
Demodulated Output Ripple:	Less than 50 mV p-p, 10 to 500 Hz (line related).
Transient Response Time:	Less than 150 μs (half load to full load to half load with a legal module filter).

RULE 3.1-2:

The maximum power available to the mainframe MSIB connectors **MUST** be specified on the mainframe's capability label.

RECOMMENDATION 3.1-3:

Mainframes should provide at least 25 watts per module slot of the mainframe. This recommendation is based on the installed base of MMS modules.

OBSERVATION 3.1-4:

When configuring an MMS system the total power requirement should be determined by adding up the power requirements of each module. The total module power requirement should not exceed the maximum power capacity of the mainframe.

OBSERVATION 3.1-5:

When configuring an MMS Mainframe predating this specification without a capability label 25 watts per module slot can be assumed when no other information is available. It is best to consult the manufacturer of an unlabeled MMS mainframe to determine its power capacity.

RULE 3.1-6:

A mainframe **MUST** be equipped with overload protection so that the 40 kHz output is not damaged by any load impedance including either a short or an open.

RULE 3.1-7:

The overload protection, when activated, **MUST NOT** cause the mainframe to exceed the normal voltage, in order to prevent damage to the system or its components.

RULE 3.1-8:

A mainframe's output voltage, during turn-on, **MUST** ramp-up monotonically in an approximately linear fashion, in 220 – 300 ms. A 3% overshoot is permissible.

OBSERVATION 3.1-9:

A mainframe with a turn-on ramp-up voltage faster than 220 ms will cause higher charging currents to the module filter capacitors and could activate the module overcurrent protection. The module overcurrent protection is typically a fuse.

RULE 3.1-10:

When driven by a 40 kHz AC waveform, the load current waveform is a modified square wave similar to that shown in figure 3-1.

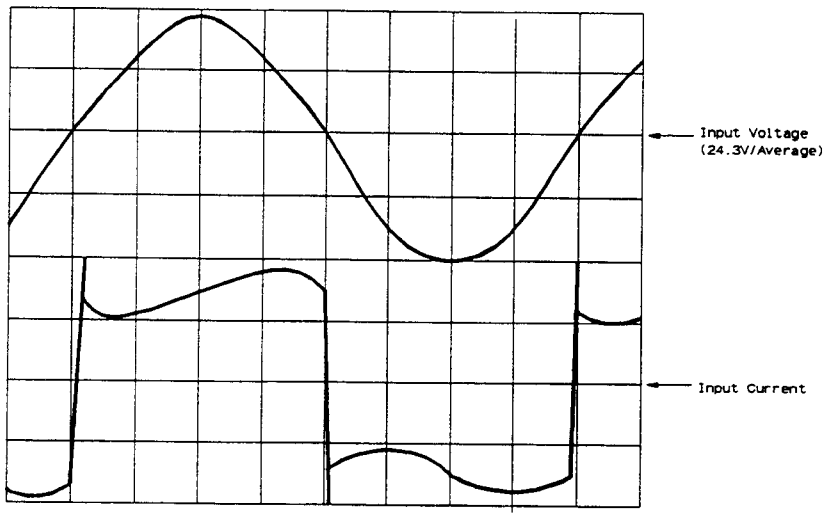


Figure 3-1. Load Current Waveform

RULE 3.1-11:
A mainframe **MUST** supply its maximum rated power under the following module conditions:

- Minimum Module Input Impedance shown in figure 3-3,
- Maximum Sideband Limits figure 3-4.

OBSERVATION 3.1-12:
Output Impedance at the mainframe MSIB connectors needs to be low enough at all frequencies to insure that any transient load changes allowed under "Load Characteristics" will not cause dynamic variations greater than specified in table 3-1. In addition, the distribution bus impedance at RF frequencies needs to be low enough to prevent conducted EMI from propagating between modules.

RULE 3.1-13:
A mainframe design **MUST** accommodate the minimum magnetizing inductance of the module power transformers. Module magnetizing inductance is specified in rule 3.2.1-1.

3.1.1 Mainframe Line Sync Output

Line Sync is derived from the AC mains. Its function is to provide a timing reference for measurements which need to be synchronized to the power line frequency.

Line Sync and Line Sync Return are delivered to the modules through the mainframe MSIB connectors. Refer to appendix A, *Connector Pin Descriptions,* for further information related to the backplane interface connector.

RULE 3.1.1-1:
The Line Sync Output circuit **MUST** have the specifications as shown in table 3-2.

TABLE 3-2. Line Sync Output Specifications

	Min	Max
V_{OH} @ I_{OH} = -0.4mA	3.75 V	5.25 V
V_{OL} @ I_{OL} = 0.4mA	0.0 V	0.4 V

OBSERVATION 3.1.1-2:
Table 3-2 translates to a minimum load impedance of 100 kΩ per slot based on an eight slot mainframe.

RULE 3.1.1-3:
The Line Sync Output **MUST** be isolated from the mainframe AC mains. An opto-isolator is recommended for this purpose.

OBSERVATION 3.1.1-4:
Line Sync is not defined for a mainframe that is powered from DC mains.

3.2 Module Power Bus Interface Specifications

OBSERVATION 3.2-1:

The mainframe 40 kHz power supply has a maximum ± 20 volts peak volts on each phase to ground. Since this is less than 42 volts, it qualifies as Safety Extra-Low Voltage (SELV). If a module generates internal voltages greater than 42 volts, it may have to meet various regulatory requirements to ensure product safety.

RULE 3.2-2:

A module, deriving power from the 40 kHz power bus, **MUST** be designed to operate from the 40 kHz power bus with the specifications listed in table 3-1.

OBSERVATION 3.2-3:

The mainframe's output voltage is specified at the mainframe MSIB connector. It does not account for losses due to the contact resistance of the interconnect. The contact resistance of the MSIB connector is a maximum of 8.3 mΩ at 3 A per pin.

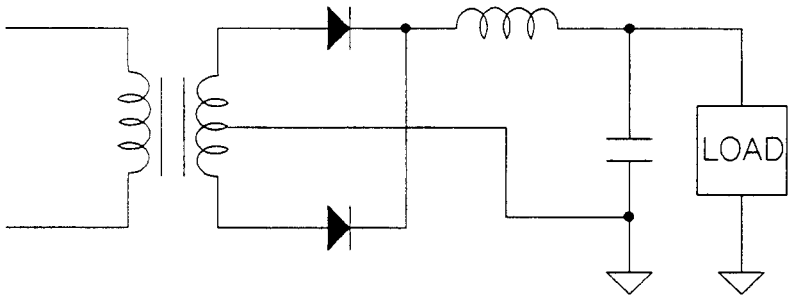


Figure 3-2. Single Output Module Supply

RULE 3.2-4:

All MMS module power supplies which derive power from the 40 kHz power bus **MUST** be transformer isolated, with full-wave rectifiers and choke inputs. Refer to figure 3-2 for an example of a single output module supply.

RULE 3.2-5:

The maximum power required by a module **MUST** be specified on the module's capability label. This is a 40kHz cycle to cycle limit as well as a long term average limit. The suggested test procedure for module power consumption is described in section B.1.1.

RULE 3.2-6:

The maximum power available through a single MSIB connector is 145 watts.

SUGGESTION 3.2-7:

For reliability and compatibility it is a good idea to limit the power used by a module. A large installed base of mainframes is available to modules that use 25 watts or less per slot.

OBSERVATION 3.2-8:

Modules built prior to this specification do not have a capability label. When configuring an MMS module without a capability label, a power requirement of 25 watts per slot width can be assumed when no other information is available. It is best to consult the manufacturer of an unlabeled MMS module to find out a module's power requirement.

RULE 3.2-9:

Each module **MUST** be equipped with primary overcurrent fault protection.

OBSERVATION 3.2-10:

The purpose of overcurrent fault protection is to prevent fires. A module's primary overcurrent fault protection is usually provided by a fuse. In the case of a module short circuit, the mainframe overcurrent may be activated before the module overcurrent fault protection (fuse) is activated. Reasonable size overcurrent fault protection for most modules is a 1 ampere rating per slot occupied by the module. The overcurrent fault device should not be oversized.

SUGGESTION 3.2-11:

Deliberate fault testing should be performed to assure that there are no conditions in which the module fuse fails to detect an overcurrent condition that has the potential to start a fire.

RULE 3.2-12:

A module deriving power from the 40 kHz power bus **MUST** use all four 40 kHz AC power pins.

RULE 3.2-13:

The maximum current through any one pin of the MSIB connector **MUST NOT** exceed 3 amps. Connector damage may occur if this limit is exceeded.

RULE 3.2-14:

Rectifiers used in the module power supplies **MUST** have a Trr, reverse recovery time of less than 200 ns.

OBSERVATION 3.2-15:

Rectifiers with Trr of less than 50 ns are readily available and strongly recommended. Rectifiers with Trr greater than 50 ns tend to cause difficulty in meeting the conducted emissions requirements of figure 8-4.

3.2.1 Module 40 kHz Power Transformer Requirements

Optimizing the transformer design will allow the maximum usable load. Restrictions have been placed on the transformer design to assure correct loading of the 40 kHz power bus.

RULE 3.2.1-1:

A module, deriving power from the 40 kHz power bus, **MUST** present the bus with an inductance equal to or greater than the lesser of :

1. $\frac{3mH}{n}$, where n is the number of slots occupied by the module, or
2. $\frac{75mH}{p}$, where p is the specified power consumption of the module, in watts.

OBSERVATION 3.2.1-2:

This inductance is typically the magnetizing inductance of the power transformer.

SUGGESTION 3.2.1-3:

Ferrite transformer core flux densities should be kept to less than 0.12 tesla. This will help limit the leakage of magnetic fields from the transformer.

OBSERVATION 3.2.1-4:

The higher the core flux level, the higher will be the radiated magnetic field generated by the power supply within the module. Note that the transformer will not be the only source of B fields. Poor printed circuit board layout can cause higher emissions than the transformer itself.

RULE 3.2.1-5:

The capacitance placed across the 40 kHz power bus by a module **MUST** be less than $0.01\,\mu F \times n$ where n is the number of slots occupied by the module.

3.2.2 Module Filter Inductor Requirements

Filter inductance is reflected back through the transformer and is seen by the 40 kHz power source control loop as part of the load. The limits on the reflected module power supply filter L and C were established with the goal of minimizing power supply load interaction between modules. Values were chosen for a reasonable mainframe power distribution system without being an excessive restraint on the module power supply design.

RULE 3.2.2-1:

The minimum reflected filter inductance **MUST** be equal to or greater than the lesser of

1. $\frac{300\mu H}{n}$, where n is the number of slots occupied by the module, or
2. $\frac{7.5mH}{p}$, where p is the specified power consumption of the module, in watts.

Figure 3-3 shows the minimum impedance for modules of various sizes, assuming they draw 25 watts per slot.

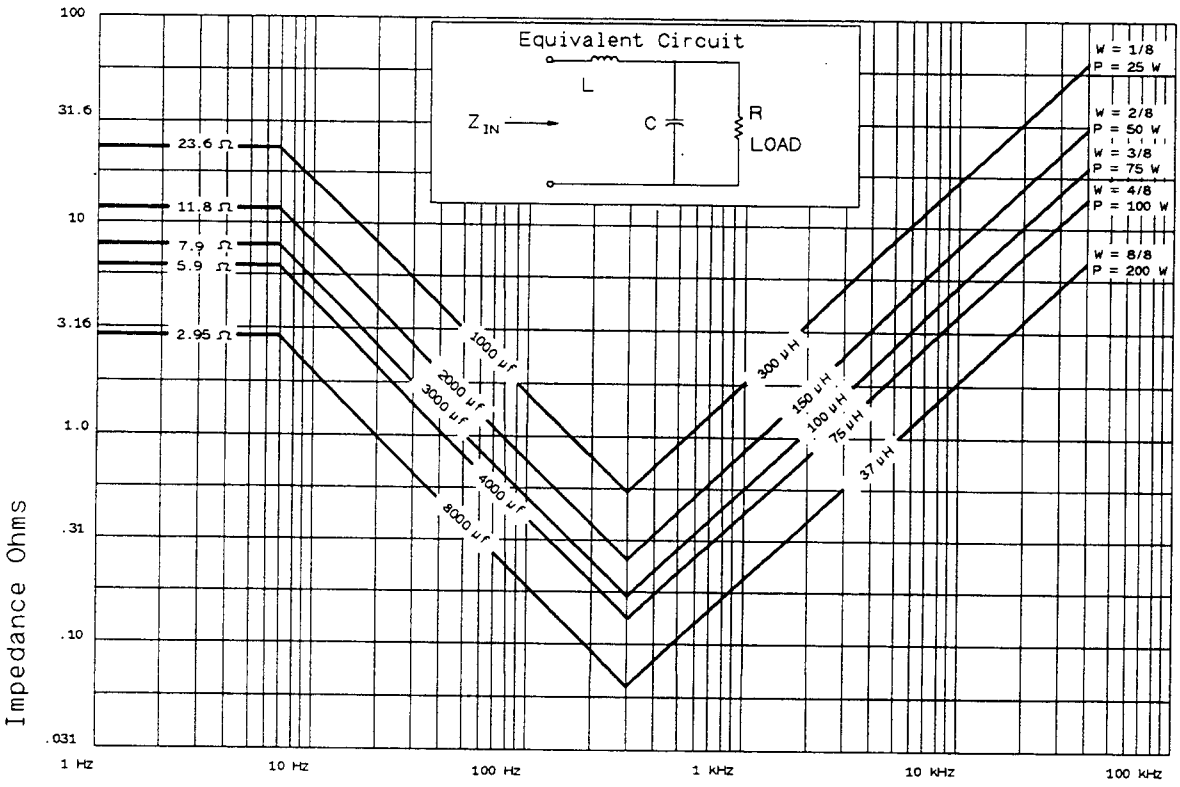


Figure 3-3. Minimum Module Input Impedance

OBSERVATION 3.2.2-2:

Module reflected filter inductance and capacitance are typically calculated from filter component values, rather than being measured directly.

RECOMMENDATION 3.2.2-3:

The maximum reflected L should be less than 2000 uH divided by the total number of slots occupied by the module.

RULE 3.2.2-4:

Each power supply filter choke **MUST** be designed so that at minimum load, the instantaneous magnetic field in the core never goes to zero.

RULE 3.2.2-5:

Filter chokes **MUST NOT** be allowed to saturate.

3.2.3 Module Filter Capacitor Requirements

Filter capacitance is reflected back through the transformer and is seen by the 40 kHz power source control loop as part of the load. The limits on reflected L and C were established with the goal of minimizing power supply load interaction between modules. Values were chosen for a reasonable mainframe power distribution system without being an excessive restraint on the module power supply design.

RULE 3.2.3-1:

The maximum reflected capacitance **MUST NOT** be greater than 1000 μF $\times$ the total number of slots occupied by the module. Refer to figure 3-3 for a minimum module input impedance graph.

RECOMMENDATION 3.2.3-2:

The minimum reflected capacitance should be greater than 100 μF $\times$ the total number of slots occupied by the module.

3.2.4 Module Load Current Variation

Variations in the amplitude of module load current are restricted in order to minimize interaction between power supplies of different modules. The restrictions are based on the characteristics of the 40 kHz power bus and the behavior of module filters. These variations can be measured by measuring the spectrum of the 40 kHz component of the current a module draws from the mainframe power supply. Load current variations will appear as sidebands on the 40 kHz component of the module's load current. The suggested test procedure for this specification is described in section B.1.2.1.

RULE 3.2.4-1:

The maximum sideband limits **MUST NOT** exceed the limits as shown in figure 3-4.

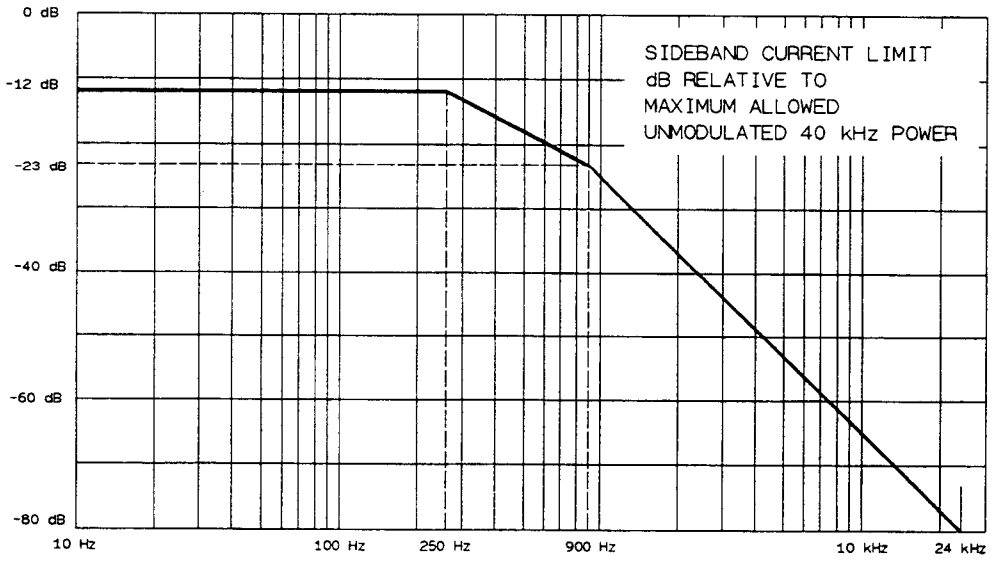


Figure 3-4. Maximum Sideband Limits

3.2.5 Module Power Supply Turn On

Turn-on delay is specified for module processor and MSIB power supplies. This specification results from the timing requirements of the MSIB interface circuits. The power supply turn-on delay is caused by the time it takes the module power supply's LC filter to become charged. In most cases, this delay specification is not a problem. This is because the module power supply regulator has enough headroom to ensure that the output will be regulated a little before the 40 kHz power supply voltage is within specification.

RULE 3.2.5-1:

The maximum turn-on delay time for a module processor and MSIB interface supply **MUST NOT** exceed 3 ms beyond the time at which the 40 kHz power bus becomes regulated (see figure 3-5).

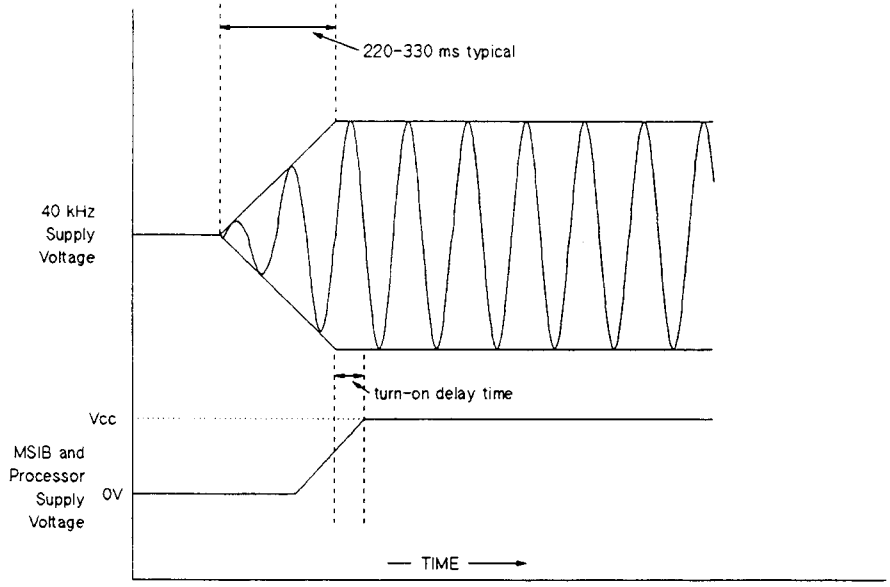


Figure 3-5. Module Power Supply Turn-on Timing

OBSERVATION 3.2.5-2:

An MMS module should expect the 40 kHz power bus, during turn on, to ramp-up in a nearly linear fashion, in 220 – 300 ms. Faster ramp-up times will cause higher charging currents to the module filter capacitors and could activate either the module or the mainframe 40 kHz power bus overcurrent fault protection.

3.2.6 Line Sync

Line Sync is available for those modules which require a timing reference for measurements which need to be synchronized to the power line frequency.

OBSERVATION 3.2.6-1:

A module is not required to use the Line Sync Output or Line Sync Return. Both lines can be terminated into open circuit when unused.

RULE 3.2.6-2:

A module using Line Sync **MUST** use both the Line Sync Output and Line Sync Return.

RULE 3.2.6-3:

A module using Line Sync **MUST** connect a minimum of 20 Ω between the Line Sync Return and module ground.

RULE 3.2.6-4:

A module using Line Sync **MUST** load the Line Sync Output with equal to or greater than 100 kΩ/n; where n is equal to the number of slots occupied by a module.

RULE 3.2.6-5:

The maximum allowable capacitance across Line Sync and return is 50 pF × n where n is the number of slots occupied by the module.

3.3 Mainframe and Module MSIB +5 Volt Supplies

MMS modules and mainframes communicate with one another via the MSIB Bus. Circuits driving the bus need to operate at the same voltage, +5 volts.

RULE 3.3-1:

The +5 volt supply used for the MSIB **MUST** be +5 ±0.25 volts.

RECOMMENDATION 3.3-2:

The use of low drop-out regulators driven by low overhead raw supplies is strongly recommended for the +5 volt supply driving the MSIB circuitry.

OBSERVATION 3.3-3:

Low drop out regulators tend to closely follow the turn on behavior of the 40 kHz bus. Tracking of the various +5 Volt power supplies that are supplying V_{cc} to the MSIB integrated circuits prevents current sourcing from one supply to the other through the MSIB integrated circuits during turn-on.

4. MODULAR SYSTEM INTERFACE BUS

The Modular System Interface Bus (MSIB) is the bus over which MMS devices communicate with each other. The Modular System Interface Bus (MSIB) defines a mechanism by which modules, mainframes, and controllers communicate. MSIB includes a mechanism for starting up communication in an orderly fashion.

RECOMMENDATION 4-1:
An MSIB interface should be implemented for logical modules which have remotely controllable functions.

4.1 Overview

The Modular System Interface Bus (MSIB) provides a means for MMS modules to communicate with each other. Any module can communicate with any other module in an MMS system independent of the rest of the modules in the system. A module may communicate both with other modules in the same mainframe and with modules in other mainframes. Communication with modules in the same mainframe is done over the MSIB internal bus. Communication with modules in other mainframes takes place over the MSIB external bus.

The basic unit of data transmission on MSIB is a packet. When a module is sending a packet to another module it does not distinguish whether that module is in the same mainframe or in another mainframe. The mainframe has the responsibility of determining whether the receiving module is in the same mainframe or not and forwarding the packet to other mainframes if it isn't.

The job of passing packets between the MSIB internal and MSIB external buses is given to a section of the mainframe called the mainframe translator. It is the translator's responsibility to watch the MSIB internal bus for packets that are not acknowledged by any modules in that mainframe and sending those packets off to other mainframes. The translator also has the responsibility of taking packets from other mainframes and sending them to modules in its mainframe.

Use of the MSIB internal bus is controlled by a section of the mainframe known as the arbiter. The arbiter has the responsibility of dividing the bandwidth of the MSIB internal bus between modules wishing to communicate over that bus. The arbiter will also allocate time to the mainframe when the translator has packets from another mainframe.

4.1.1 Address Space

MMS Modules reside in the MSIB address space. This space is made up of 256 unique addresses. These addresses are only unique, however, within a local MSIB network.

Each address in the local MSIB network may be either vacant or occupied by a module.

4.1.1.1 Vacant Address

A module sending data to a vacant address will receive an indication that there is no module present at that address.

It is possible to build hardware that can receive data sent to a vacant address without responding in any way (BSY or ACK). Multiples of these receivers could be set to the same address, thereby allowing transmissions to multiple receivers at the same time. The details on how to do this are not covered in this document.

4.1.1.2 Occupied Address

Data sent to an address occupied by a module will be received by that module. If the module is busy then the sending module will resend the data until the module can receive it.

4.1.2 Packets

As stated above, the basic unit of data transmission on MSIB is a packet. A packet is made up of 8 fields totaling 36 bits. The order in which these fields are transmitted is dependent on the particular bus (internal or external) over which they are sent. The fields are grouped into frames, each frame consisting of one 8 bit field and one 1 bit field.

TABLE 4-1. Packet Contents

Frame	Field	Bits	Description
TO	TO ADDRESS	8	MSIB address of destination module
	B/W	1	Byte/word: 1=byte, 0=word
FROM	FROM ADDRESS	8	MSIB address of source module
	EA	1	external acknowledge (see below)
D1	DATA 1	8	First data byte
	NA	1	Not accepted (see below)
D2	DATA 2	8	Second data byte
	CMD	1	Command flag: 1=command, 0=data

The TO Address and FROM Address fields of a packet contain the MSIB addresses of the receiver and sender of the packet. The Data 1 and Data 2 fields contain the two bytes of data that the packet is sending. The B/W field is used to indicate whether the packet contains one or two bytes of data. The CMD field indicates whether the data fields contain data or whether they contain an MSIB command. For more information on the use of the B/W and CMD fields see chapter 5, *Communication Protocol.* The EA and NA fields indicate whether a receiver was found for the packet and whether that receiver was able to accept the packet.

4.1.3 Reset

In a system containing many modules, some of which are parts of instruments made up of many modules, it is important that the system start running in an orderly fashion. Specifically, it is important that all modules start running at the same time so that modules that control groups of other modules can determine where the other modules reside in the system and configure themselves appropriately.

This is accomplished by a mechanism that is made up of part hardware and part protocol. The hardware portion of that mechanism, known as the reset mechanism, will be described in this chapter. The protocol portion is discussed in chapter 5, *Communication Protocol.*

The reset mechanism is global to the system; a reset signal generated in any part of the system will affect all modules in the system.

A reset signal may be generated either by a mainframe or by a module. When a mainframe is powered down it will indicate a reset condition to other mainframes over the MSIB external bus. When a mainframe is powered up but the power supply to the modules is not within the specified range the mainframe will indicate reset to other mainframes and to modules within that mainframe. Once a mainframe has released its own reset and determined that other mainframes have released reset it will release reset to its modules.

After the mainframe has released reset to the modules a module may assert reset on the MSIB internal bus. This has two affects: First, it puts the other modules in that mainframe into reset. Second, the signal is detected by the MSIB mainframe translator and sent to other mainframes. The result is that the system is placed into reset. When the module releases the MSIB internal bus reset the system is released from reset (provided no other component is holding the system in reset). For more information on reset see section 4.2.1.1.7 and section 4.3.5.

4.2 MSIB Internal Bus

MSIB communication takes place over two different buses. Communication between modules that reside in the same mainframe takes place over the MSIB internal bus. Communication between mainframes is done on the MSIB external bus. A message from a module in one mainframe to a module in another mainframe goes first from the sending module to its mainframe over the MSIB internal bus. It then goes over the MSIB external bus from that mainframe to the mainframe that has the receiving module. Finally, it goes over the MSIB internal bus in that mainframe to the receiving module.

This section describes communications on the MSIB internal bus.

4.2.1 Overview

Data is sent over the MSIB internal bus as a series of packets. The arbiter allocates time slots to modules and the mainframe during which packets are sent. These time slots are allocated as needed on a packet by packet basis. A module or the mainframe requests a time slot by asserting its RTS line. The arbiter grants the request by asserting the corresponding CTS line.

Packets are sent as a sequence of frames. Each frame is sent during the time between one falling edge of the clock and the next. A packet will take between two and four frames to transmit. A complete packet will take four times but in some cases the packet may be terminated after two or three frames. Figure 4-1 shows the transmission of a typical packet.

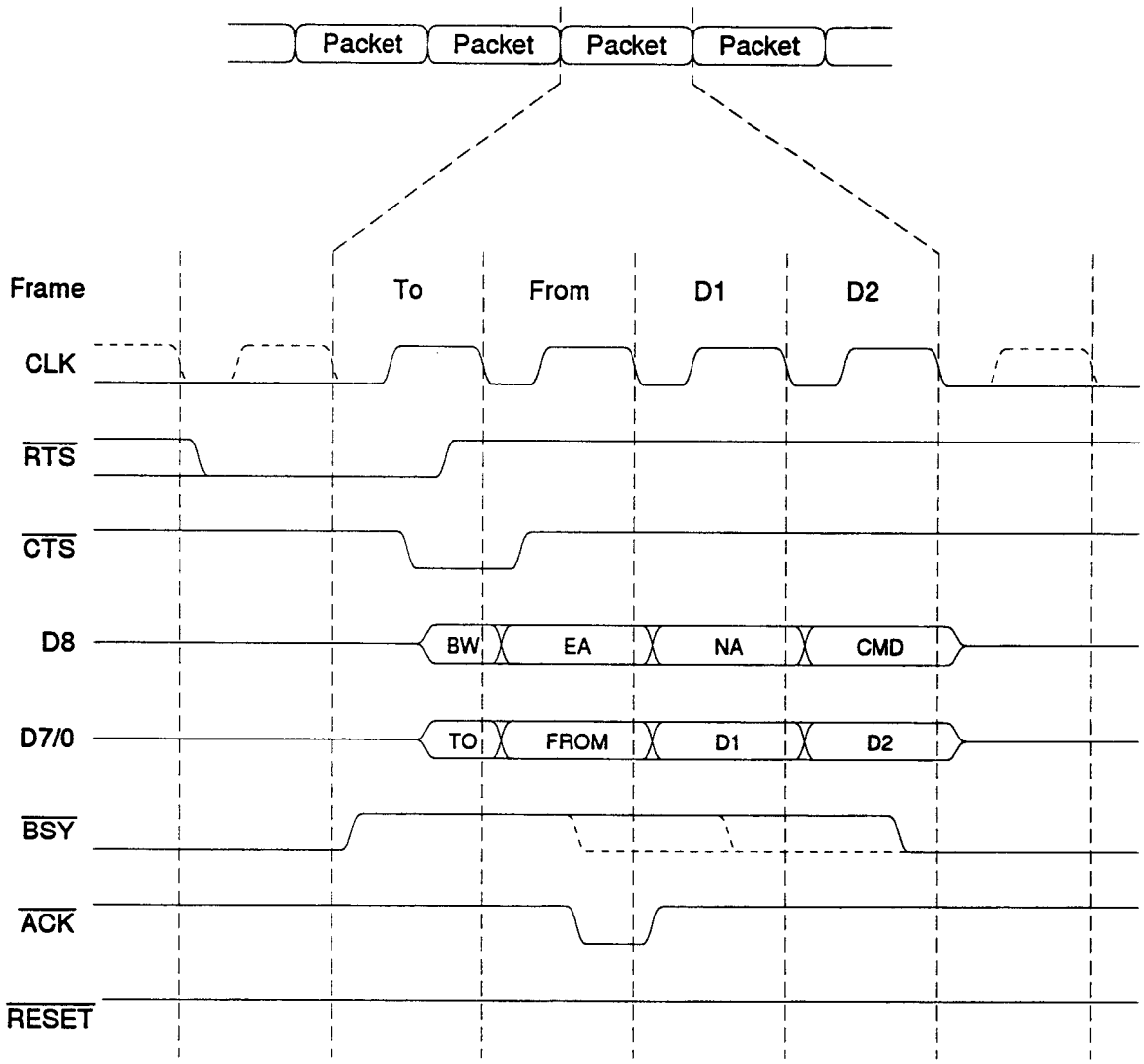


Figure 4-1. Transmission of a Typical Packet

A packet transmission is initiated by a module or the mainframe translator asserting its RTS line. The mainframe responds to this by starting a packet and asserting CTS to the module or mainframe that asserted its RTS.

The mainframe starts a packet by starting the clock and releasing BSY. The CLK line is only active when a packet is being sent. It is held low at all other times. BSY being unasserted indicates the start of a packet. A frame in which BSY is unasserted following a frame in which BSY is asserted is the first frame of a packet, the TO frame. The assertion of BSY terminates the packet. The frame in which

BSY is asserted is the last frame of the packet.

The assertion of CTS to a module causes that module to drive the first frame of the packet onto the bus. During succeeding clock periods the module drives the rest of the frames onto the packet. If the receiver of the packet is present on the bus it will assert the ACK line during the FROM frame. If ACK is not asserted in the FROM frame the mainframe translator will send the packet off to other mainframes. If the receiver is present but unable to accept the packet (probably because its input buffer is full) it will assert BSY in either the FROM or D1 frame. If the receiver does not assert BSY in either the FROM or D1 frame then the mainframe will assert BSY in the D2 frame to complete the packet.

4.2.1.1 Signals

The MSIB internal bus consists of the following signals:

TABLE 4-2. MSIB Internal Bus Signals

Name	Driven by	Type	Assertion Level	Description
CLK	Mainframe	Sing		Backplane clock
D8	Mainframe or Module	Tri	positive logic	Data line 8
D7-0	Mainframe or Module	Tri	positive logic	Data lines 7 through 0
RTS	Module	Sing	active low	Request to send
CTS	Mainframe	Sing	active low	Clear to send
BSY	Mainframe or Module	Pre	active low	Busy
ACK	Mainframe or Module	Pre	active low	Acknowledged
RESET	Mainframe or Module	Open	active low	Bus reset

Type:

Sing	Single ended
Tri	Tri-state
Pre	Open collector - Pre-charged
Open	Open collector - Passive pullup

All MSIB internal bus signals are common to all the modules with the exception of RTS and CTS. There is one RTS and one CTS signal connecting each module with the arbiter.

The BSY and ACK signals are pre-charged to a logic high level during the first portion of each clock cycle. During the last portion of the clock cycle they are passively held high. During this time they may be pulled low to signal a condition. This gives them the wire-or function of passive pullup open collector without the speed limitations.

All timing rules of the MSIB internal bus apply to signals at the MSIB connector.

4.2.1.1.1 CLK

CLK is the signal to which all other signals on the MSIB internal bus are referenced. An MSIB internal frame spans the period between two high to low edges of this signal.

The CLK signal is only active when the bus is in use. When the bus is idle the clock is stopped.

4.2.1.1.2 D8 Through D0

The signals D7 through D0 are used to transmit the four 8 bit fields of a packet. The signal D8 is used to transmit the four 1 bit fields of a packet. These signals are driven and received by the components that transfer data: the mainframe translator and the modules. The arbiter does not drive or receive these signals.

4.2.1.1.3 RTS

This signal is used by a module or the mainframe translator to request a time slot from the arbiter. If the bus is inactive this signal will cause the mainframe to start the clock.

4.2.1.1.4 CTS

This signal is used by the arbiter to inform a component that it has been granted a time slot on the bus.

4.2.1.1.5 BSY

The BSY signal is the synchronizer of frames on the bus. A frame in which BSY is not asserted following a frame in which BSY is asserted indicates the start of a packet. This frame is the first (TO) frame of the packet. The packet progresses until BSY is asserted. The frame in which BSY is asserted becomes the last frame of the packet. All subsequent frames are idle frames until BSY is again released.

The frame in which BSY is asserted determines the status of the packet. BSY asserted in FROM or D1 indicates a receiver is busy. This indicates the need to re-transmit the packet. In this case it is the receiver that asserts BSY. BSY asserted in D2 indicates the normal completion of the packet. In this case it is the mainframe that asserts BSY.

RULE 4.2.1.1.5-1:

A component **MUST** only assert BSY if it is to continue to assert it through the remainder of the frame.

4.2.1.1.6 ACK

The ACK signal is used by a module to signal a match between its MSIB address and an address field (TO or FROM) of a packet. The match is signaled by the assertion of ACK in the frame following the frame that contained the matching address.

The receiver of a packet will use ACK to signal a match between its address and the TO field of a packet. It will do this by asserting ACK in the FROM frame of the packet. This is a signal to the sender of the packet and to the mainframe translator that the receiver is present in the mainframe. A packet for which ACK is not asserted in the FROM frame will be passed on to other mainframes by the mainframe translator.

The sender of a packet will assert ACK in the D1 frame to indicate that its address matches the FROM field of the packet. It does not do this when it is sending a packet but only when the mainframe translator is returning a packet that has been sent to other mainframes. This is an indication to the mainframe translator that the packet has returned to the sender and should not be forwarded to the next mainframe.

RULE 4.2.1.1.6-1:

A component **MUST** only assert ACK if it is to continue to assert it through the remainder of the frame.

4.2.1.1.7 RESET

The MSIB internal bus RESET signal is used to indicate or initiate a system reset. When this signal is asserted it is an indication to all modules that the system is in reset. The signal may be asserted by either the mainframe or by a module. If it is asserted by a module then it is an indication to the mainframe that the system is to be put into reset.

The mainframe will assert RESET either when it is powering up or down (the power supplied to the modules is not within the specified range) or when its mainframe translator detects a reset signal initiated from outside this mainframe (e.g., from another mainframe). A module will assert RESET in order to reset the system. See sections 4.2.2.3 and 4.2.3.4 for more detail.

RULE 4.2.1.1.7-1:

Any component asserting RESET **MUST** assert it for a minimum of 100 ms.

4.2.1.1.8 Precharge and Pullup

Each of the signals BSY and ACK is a pre-charged signal. That is, it is pulled high by the mainframe during the first part (CLK low) of a frame. During the second part of the frame it may be pulled low by either the mainframe or a module. If neither the mainframe nor a module pulls it low then it will be held high by the bus termination resistors and sensed as a high at the end of the frame.

4.2.1.1.9 Timing

The timing of the signals on the MSIB internal bus is shown in figure 4-2. The timing values are listed in table 4-3.

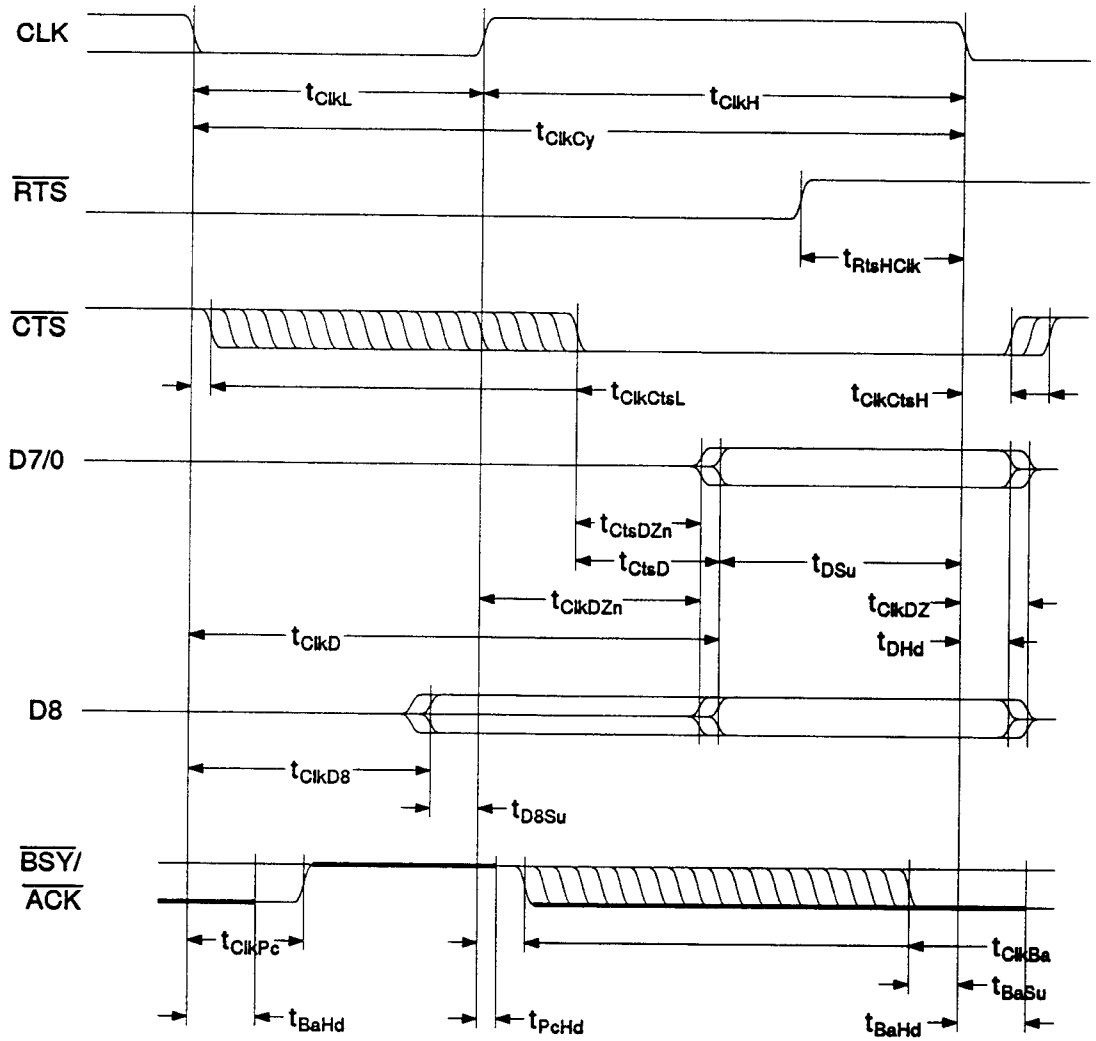


Figure 4-2. Timing of Signals on the MSIB Internal Bus

TABLE 4-3. Timing Values of Signals on the MSIB Internal Bus

Symbol	R	Frame	Min	Max	Notes	Description
ClkCy	D	All	161	162		Clock cycle time
ClkL	D	All	60	-	A	Clock low time
ClkH	D	All	80	-	A	Clock high time
ClkSkew	D	All	-	10		Clock skew between any two modules
RtsHClk	D	TO	0	-		RTS release to Clock
ClkCtsL	D	TO	25	75		Arbiter Clock to assert CTS
ClkCtsH	D	TO	-	75		Arbiter Clock to release CTS
CtsDZn	D	TO	0	-		CTS low to data drive
ClkDZn	D	TO	0	-		CLK high to data drive
ClkDZ	D	Last	-	30		Driver delay before releasing data lines
CtsD	D	TO	-	45	B	CTS true to data TO/BW valid
ClkD	D	FROM	-	100	B	Clock low to data FROM valid
	D	D1	-	135	B	Clock low to data D1 valid
	D	D2	-	135	B	Clock low to data D2 valid
DSu	R	TO	-	40		Receiver data TO/BW setup requirement
	R	FROM	-	60		Receiver data FROM setup requirement
	R	D1	-	25		Receiver data D1 setup requirement
	R	D2	-	25		Receiver data D2 setup requirement
DHd	D	All	15	-		Driver data hold time
	R	All	-	5		Receiver data hold requirement
ClkD8	D	FROM	-	45		Clock to data EA valid
	D	D1	-	45		Clock to data NA valid
	D	D2	-	45		Clock to data CMD valid
D8Su	R	FROM	-	5		Receiver data EA to Clock high setup req.
	R	D1	-	5		Receiver data NA to Clockhigh setup req.
	R	D2	-	5		Receiver data CMD setup requirement
ClkPc	D	All	35	-		Clock low to precharge start
PcHd	D	All	0	5		Clock high to precharge end
ClkBa	D	All	15	-		Clock high to BSY/ACK assert
BaSu	R	All	-	35		Receiver BSY/ACK setup requirement
BaHd	D	All	10	25		Driver BSY/ACK hold
	R	All	-	0		Receiver BSY/ACK hold requirement

Notes:

(A) This translates to a duty cycle in the range of 37.3% to 50.0%.
(B) These values are observations only. They are derived from other values in this table.

The columns of the table are defined as follows:

Symbol:	Time subscript from figure 4-2.
R:	Indicates who is responsible for this parameter. D: The driver of the signal; R: The receiver of the signal.
Frame:	Indicates which frame(s) this value applies to.
Min:	Minimum allowable time in ns.
Max:	Maximum allowable time in ns.
Description:	A brief description.

RULE 4.2.1.1.9-1:
The times described above **MUST** be met for all components on the MSIB internal bus.

4.2.1.1.10 Transceivers
The requirements for drivers and receivers are shown in the following table.

TABLE 4-4. MSIB Internal Bus Transceiver Characteristics

Symbol	Parameter	Min	Max		Conditions
V_{TH}	High-Level Input Threshold Voltage		2.0	V	
V_{TL}	Low-Level Input Threshold Voltage	0.8		V	
V_{OH}	High-level Output Voltage	2.7	5.25	V	I_0 = -0.4 mA
V_{OL}	Low-level Output Voltage	-0.5	0.5	V	I_0 = 16 mA
I_{IH}	High-level Sink Current		20	μA	V_I = 2.7 V
I_{IL}	Low-level Source Current		-0.1	mA	V_I = 0.4 V

RULE 4.2.1.1.10-1:
All transmitters and receivers on the MSIB internal bus **MUST** meet the requirements shown in table 4-4.

RECOMMENDATION 4.2.1.1.10-2:
Module transmitters and receivers should be located as close as possible to the MSIB connector.

OBSERVATION 4.2.1.1.10-3:
Since driver characteristics determine the bus settling time it is important that drivers be chosen to insure that bus signals settle within the specified time.

4.2.2 Module
The module interface is the module's connection to the MSIB internal bus.

A module interface is made up of three sections:

- **Transmit** - Transmit packets onto internal bus
- **Receive** - Receive packets from internal bus
- **Reset** - Assert/Sense reset signal from internal bus

4.2.2.1 Module Transmit
The purpose of the transmit section is to send a packet from the module in which it resides to the receive section of another module by way of the internal bus and possibly the external bus. It does this by requesting a time slot on the internal bus from the arbiter and then transmitting the packet onto the bus when the request is granted. The transmit section must recognize when a packet has been forwarded by the mainframe translator and wait for that packet to be returned.

When a module has a packet to send it asserts RTS. The arbiter will respond by asserting CTS, allowing the module to send the packet.

4.2.2.1.1 Module Transmit Algorithm

The module transmitter algorithm is described in figures 4-3 and 4-4. The algorithm description uses the state machine notation defined in section 1.4.3. This description is not intended as an implementation of the algorithm. An actual implementation would quite likely differ from the state machine shown here. For example, a single state in this description may be implemented as multiple states. All state transitions occur on the high to low transition of CLK.

The algorithm consists of two state machines. The machine in figure 4-3, the send machine, sends a packet from the module onto the internal bus. The machine in figure 4-4, the return machine, removes packets from the internal bus that were sent over the external bus by the mainframe and notifies the send machine when this occurs.

When RESET is asserted the send machine (figure 4-3) releases the MSIB internal data bus lines, clears the Trdy flag and enters state A.

A: The send machine remains in state A until it receives a CTS signal and it identifies the first frame of a packet. The first frame of a packet is a frame in which BSY is not asserted following a frame in which BSY is asserted. While in state A it will assert RTS if it has a packet to send, it currently has no packet on the external bus, and CTS is not asserted. When CTS is asserted the module will asynchronously release RTS and drive its TO frame data onto the data lines.

If at the end of a frame, CTS is asserted, the frame is the first frame of a packet, there is a packet to be sent, and the module does not have a packet on the external bus, then the module will proceed to state B to send the FROM frame data.

If CTS is asserted at the end of the TO frame but the module either has no packet to send or has a packet on the external bus then it proceeds to state G where it will terminate the packet.

B: The send machine remains in state B for the duration of the FROM frame. In state B the module drives the data lines with its FROM frame data. If BSY is asserted at the end of the FROM frame the receiver was busy and the send machine will return to state A to re-try sending the packet. If BSY is not asserted at the end of the frame then the send machine will check ACK. If ACK is asserted then the receiver is in the same mainframe and the packet will not be sent to the external bus. The module will proceed to state C. If ACK is not asserted then the receiver is not in the same mainframe and the packet is going to be sent to the external bus. The module will proceed to state E.

C: The send machine remains in state C for the duration of the D1 frame. In state C the module drives the data lines with its D1 frame data. If BSY is asserted at the end of the D1 frame the send machine will return to state A and wait for the next packet to start. If BSY is not asserted at the end of the frame then the send machine will check ACK. If ACK is not asserted in the D1 frame the module will proceed to state D to complete the packet. If ACK is asserted then the send machine will assume the packet will be sent to the external bus and will go to state F to complete the packet.

D: The send machine remains in state D for the duration of the D2 frame. In state D the module drives the data lines with its D2 frame data. At the end of the D2 frame the send machine will return to state A to await the start of the next packet.

E: In state E, as in state C, the packet is in the D1 frame and the module is driving the data bus with its D1 frame data. In state E, however, the module has determined that the destination module is not in this mainframe and therefore the packet will be sent to the external bus. If the packet is terminated in the D1 frame by a BSY signal the send machine will return to state A to re-send the packet. Otherwise it will continue to state F to finish the packet.

F: In state F, as in state D, the packet is in the D2 frame and the module is driving the data bus with its D2 frame data. In state E, however, the module has determined that the destination module is not in this mainframe and therefore the packet will be sent to the external bus. On leaving the

F state the module sets the PktExt flag indicating that the module has a packet on the external bus.

G: State G is entered when the module received a CTS but has no packet to send. The module remains in state G for the duration of the FROM frame but does not drive the data bus. If BSY is asserted at the end of the FROM frame then the module returns to state A. Otherwise the module continues to state H where it will assert BSY to terminate the packet.

H: In state H the module asserts the BSY signal but does not drive the data lines. The assertion of BSY in the D1 frame will terminate the packet.

Return portion of the module send state machine deals with the return packets that were sent to the external bus.

K: The module will remain in state K until it sees a TO frame with no CTS. This lets it track all packets except the packets it is sending. Once it sees the state of a packet that it is not sending it proceeds to state L.

L: The module remains in state L for the FROM frame of the packet. The module will return to state K at the end of the FROM packet if either BSY is asserted or the data in the FROM address of the packet does not match the module's address. If the data in the FROM field of the packet matches the module's address then the packet is being returned from the external bus. The module proceeds to state M for the D1 frame.

M: The module remains in state M for the D1 frame. While in state K the module asserts the BSY and ACK signals. The BSY signal terminates the packet in the D1 frame. The ACK signal indicates to the mainframe that the packet has returned to the sender and should not be passed back to the external bus. At the end of the D1 frame the module will clear the PktExt flag, indicating that it no longer has a packet on the external bus. If either of the EA or NA bits of the packet are clear the module will clear the Trdy flag, indicating that there is no longer a packet to be sent. The EA bit being clear indicates that a destination module for the packet was not found. If the EA bit is set but the NA bit is not set then the destination module was found and accepted the packet. If both bits are set then the destination was found but was not able to accept the packet. In this case the Trdy flag is not cleared, which will result in the packet being re-sent.

RULE 4.2.2.1.1-1:

A module transmitter **MUST** implement states A through F of figure 4-3 and states K through M of figure 4-4.

RECOMMENDATION 4.2.2.1.1-2:

A module transmitter should implement states G and H of the module transmitter algorithm (figure 4-3). These states will normally not be executed, but they prevent an errant CTS from generating an invalid MSIB packet.

OBSERVATION 4.2.2.1.1-3:

If the EA bit of the returning packet is clear then there is no module at the TO address.

PERMISSION 4.2.2.1.1-4:

A module transmitter may assert RTS for the duration of a packet if it has another packet to send that can be sent immediately following the current one. In this case RTS remains asserted when CTS becomes true in state A.

PERMISSION 4.2.2.1.1-5:

A module transmitter may abort a transmission on any transition that would go to state A by following the normal transition actions and clearing Trdy.

PERMISSION 4.2.2.1.1-6:

A module transmitter may abort a transmission while in state A by releasing RTS, provided that it implements states G and H.

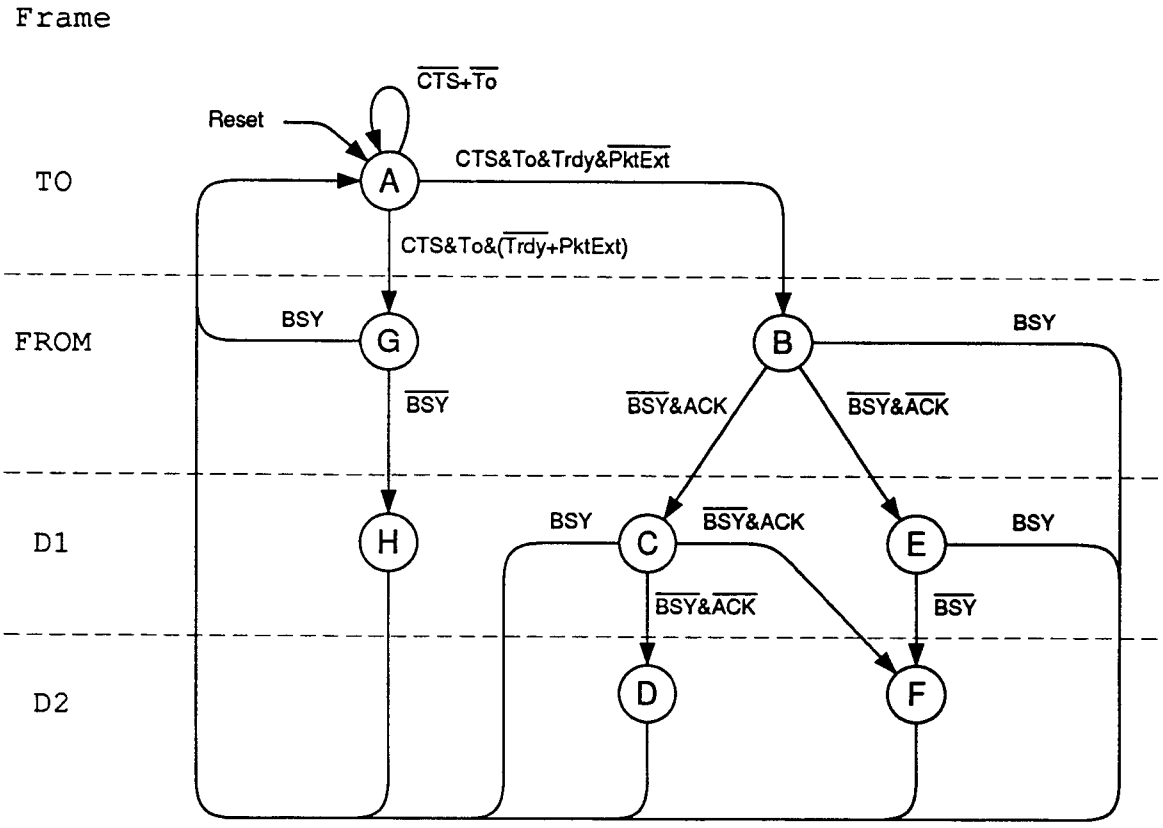


Figure 4-3. Module Transmit Algorithm-Send

TABLE 4-5. Module Transmit Algorithm-Send Notation

States:

A	Idle or TO frame
B	Sending FROM frame of packet
C	Sending D1 frame - receiver in same mainframe
D	Sending D2 frame (internal)
E	Sending D1 frame - receiver not in same mainframe - packet going external
F	Sending D2 frame (external)
G	Errant CTS from Arbiter
H	Terminate packet in D1

Conditions:

ACK	MSIB internal bus ACK signal
BSY	MSIB internal bus BSY signal
CTS	Clear TO Send signal from Arbiter
MA	Value clocked from data lines matches my address
NA	NA (Not Accepted) bit in packet - Receiver was busy
PktExt	The packet in on the external loop
Reset	MSIB internal bus RESET signal
TO	TO frame - frame with BSY false following frame with BSY true
Trdy	State of Trdy flag latched on rising edge of CLK (see observation 4.2.2.1.1-7)

Outputs:

State	BSY	Drive TO	Drive FROM	Drive D1	Drive D2	Clear Trdy	Set PktExt	RTS
A	-	if CTS	-	-	-	-	-	if ready
B	-	-	drive	-	-	-	-	-
C	-	-	-	drive	-	-	-	-
D	-	-	-	-	drive	enable	-	-
E	-	-	-	drive	-	-	-	-
F	-	-	-	-	drive	-	enable	-
G	-	-	-	-	-	-	-	-
H	assert	-	-	-	-	-	-	-

BSY	-	do not assert BSY
	assert	assert BSY during the CLK low time of this frame
Drive TO	-	do not drive data lines with TO frame data
	if CTS	drive data lines with TO frame data while CTS is asserted
Drive FROM	-	do not drive data lines with FROM frame data
	drive	drive data lines with FROM frame data
Drive D1	-	do not drive data lines with D1 frame data
	drive	drive data lines with D1 frame data
Drive D2	-	do not drive data lines with D2 frame data
	drive	drive data lines with D2 frame data
Clear Trdy	-	do not clear Trdy flag
	enable	clear Trdy flag at the end of this frame
Set PktExt	-	do not set PktExt flag
	enable	set PktExt flag at the end of this frame
RTS	-	do not assert RTS
	if ready	assert RTS while Trdy flag is set, PktExt flag is not set, and CTS is not asserted

OBSERVATION 4.2.2.1.1-7:

Since the Trdy flag can change asynchronous to the MSIB Internal bus clock it is necessary to synchronize it by latching it on the rising edge of the clock. This latched signal is then input to the state machine.

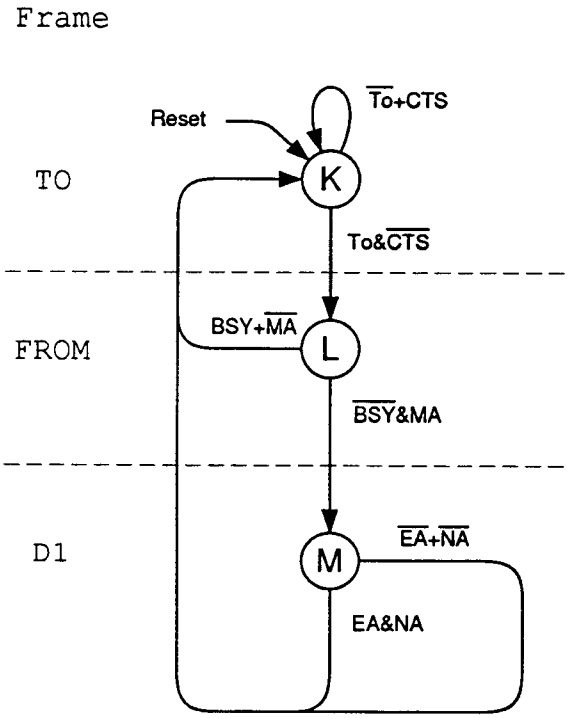


Figure 4-4. Module Transmit Algorithm-Return

TABLE 4-6. Module Transmit Algorithm-Return Notation

States:				
K	Idle or TO frame			
L	FROM frame - check for returning packet			
M	My packet - ACK and terminate it			
Conditions:				
BSY	MSIB internal bus BSY signal			
CTS	Clear TO Send signal from Arbiter			
EA	Packet has EA flat set (D8 in FROM)			
MA	Value clocked from data lines matches my address			
NA	NA (Not Accepted) bit in packet - Receiver was busy			
Reset	MSIB internal bus RESET signal			
TO	TO frame - frame with BSY false following frame with BSY true			
Trdy	State of Trdy flag latched on rising edge of CLK			
Outputs:				
State	**BSY**	**ACK**	**Clear Trdy**	**Clear PktExt**
K	-	-	-	-
L	-	-	-	-
H	assert	assert	if done	enable
BSY	-	do not assert BSY		
	assert	assert BSY during the CLK low time of this frame		
ACK	-	do not assert ACK		
	assert	assert ACK during the CLK low time of this frame		
Clear Trdy	-	do not clear Trdy flag		
	if done	clear Trdy flag at the end of this frame if either the EA or NA bits of the packet are clear		
Clear PktExt	-	do not clear PktExt flag		
	enable	clear PktExt flag at the end of this frame		

4.2.2.1.2 Signals

RULE 4.2.2.1.2-1:
The module MSIB internal bus transmitter **MUST NOT** assert BSY in the TO, FROM, or D2 frames of a packet.

RULE 4.2.2.1.2-2:
The module MSIB internal bus transmitter **MUST** drive RTS at all times. RTS is not a tri-state or open collector line.

OBSERVATION 4.2.2.1.2-3:
Note that the conditions set forth in section 4.2.1.1 apply here.

4.2.2.1.3 Timing

RULE 4.2.2.1.3-1:
The following parameters as described in figure 4-2 and table 4-3 **MUST** be met by a module's MSIB internal transmitter:

BaHd	BaSu	ClkBa	ClkD	ClkD8	ClkDZn
CtsD	CtsDZn	D8Su	DHd	DSu	

4.2.2.2 Module Receive

The purpose of the Receive section is to receive packets sent to a module. It does this by watching the internal bus for a packets with a TO address that match its own and extracting the data from such packets.

4.2.2.2.1 Module Receive Algorithm

The module receiver algorithm is described in figure 4-5. The algorithm description is in the form of a state machine as defined in section 1.4.3. This description is not intended as an implementation of the algorithm. An actual implementation would quite likely differ from the state machine shown here. For example, a single state in this description may be implemented as multiple states. All actions of the module receiver occur on the high to low transition of CLK. A module receiver never drives the internal bus data lines.

The receive portion of a module does not drive the data lines. On RESET the receive state machine enters state A.

A: In state A the module waits for a packet to start (the TO frame). When the module detects the TO frame it checks whether the data in the TO field of the packet matches its address. If it does not the module remains in state A. If the TO address does match its own address then the module checks whether it has room in its receive buffer to accept the packet. If it does not then it will proceed to state F where it will terminate the packet. If it does have room then it will store the data from the TO frame data of the packet and will continue to state B.

B: The module remains in state B for the FROM frame. In this frame the module asserts ACK to indicate that it (the destination module) is present on the bus. If at the end of the FROM frame the module detects that the EA bit in the packet is set it must assume that the packet has already been received and therefore should not be received again. In this case the module returns to state A to await the next packet.

It is possible for a module to reject a packet at the end of the FROM frame as well as the end of the TO frame. This will most likely occur because for some reason the module does not want to accept the packet based on its FROM address. To do this the module proceeds to state E where it will terminate the packet. Otherwise the module will latch the data from the FROM frame of the packet and proceed to state C.

C: The module remains in state C for the D1 frame of the packet. If at the end of the frame the BSY signal is set the module will return to state A to await the start of the next packet. Otherwise at the end of the frame the module will latch the D1 frame data and continue to state D.

D: The module remains in state D for the D2 frame of the packet. At the end of the D2 frame the module will latch the D2 frame data and set a flag (Rfull) indicating a packet has been received. At the end of the D1 frame the module returns to state A to await the next packet.

E: The module enters state E in the D1 frame of a packet when it is rejecting the packet. In state E the module asserts BSY to terminate the packet. At the end of the D1 frame the module returns to state A to await the next packet.

F: A module will enter state F in the From frame of a packet if it is unable to accept the packet because its input buffer is full. In state F the module asserts ACK to indicate that it (the destination module) is present on the bus and asserts BSY to terminate the packet. At the end of the From frame the module returns to state A to await the next packet.

RULE 4.2.2.2.1-1:
A module receiver **MUST** implement states A through E of the module receive algorithm (figure 4-5).

RECOMMENDATION 4.2.2.2.1-2:
A module should implement the state transition from B to A. This transition will normally not occur, but it provides a more robust implementation.

PERMISSION 4.2.2.2.1-3:
A module receiver may omit the state transition from B to A.

PERMISSION 4.2.2.2.1-4:
A module receiver may omit latching the TO address at the end of the TO frame.

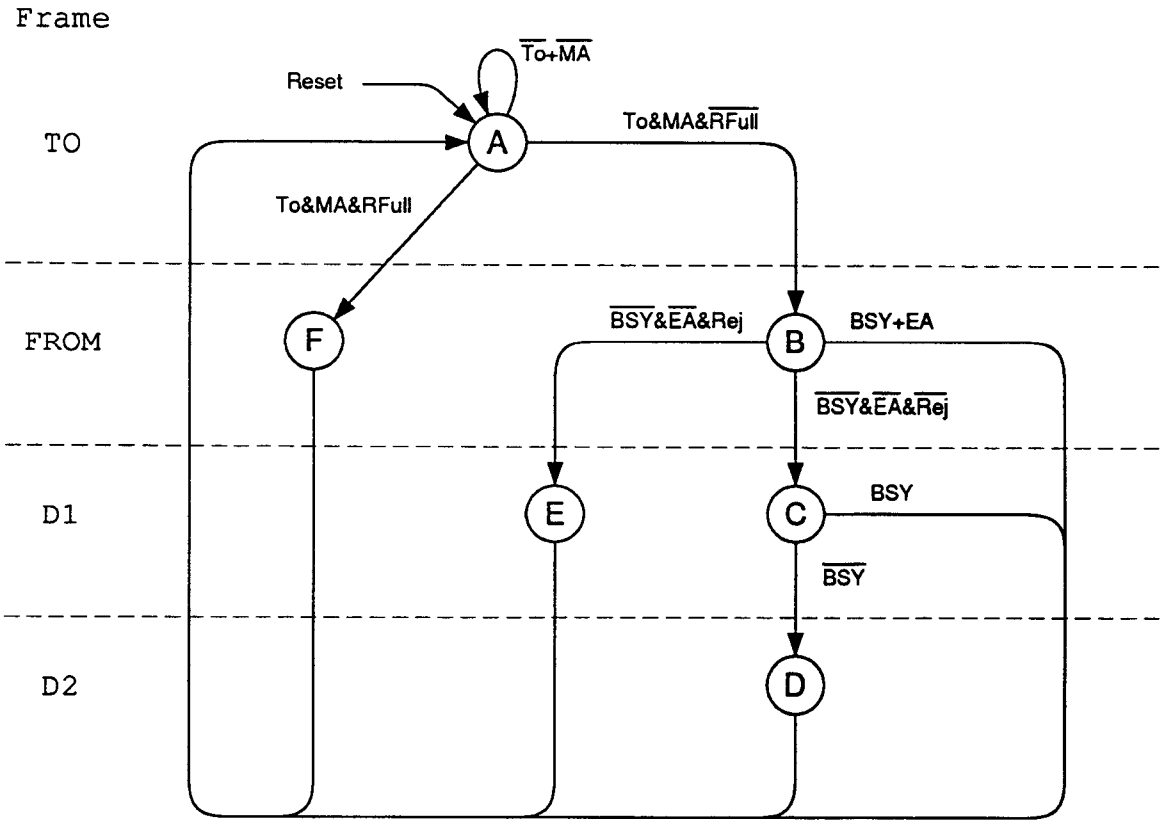


Figure 4-5. Module Receive Algorithm

TABLE 4-7. Module Receive Algorithm Notation

States:

A	Idle or TO frame
B	Got TO address, it is for me, and I can accept it
C	Got FROM address, I can accept it, now get D1
D	Got D1, now get D2
E	It is for me but the packet is being rejected
F	It is for me but I cannot accept it, asserting BSY

Conditions:

BSY	MSIB internal bus BSY signal
EA	Packet has EA flat set (D8 in FROM)
MA	Value clocked from data lines matches my address
Rej	Reject packet with this FROM address
Reset	MSIB internal bus RESET signal
TO	TO frame - frame with BSY false following frame with BSY true
RFull	State of RFull flag latched on rising edge of CLK (see observation 4.2.2.2.1-5)

Outputs:

State	BSY	ACK	Latch TO	Latch FROM	Latch D1	Latch D2	Set RFull
A	-	if not RFull	-	-	-	-	
B	-	assert	-	enable	-	-	-
C	-	-	-	-	enable	-	-
D	-	-	-	-	-	enable	enable
E	assert	-	-	-	-	-	-
F	if nEA	assert	-	-	-	-	

BSY	-	do not assert BSY
	assert	assert BSY during the CLK low time of this frame
	if nEA	assert BSY during the CLK low time of this frame if the EA bit of the packet is clear
ACK	-	do not assert ACK
	assert	assert ACK during the CLK low time of this frame
Latch TO	-	do not latch TO frame data from data lines
	if not RFull	latch TO frame data from the data lines at the end of this frame if the latched value of the RFull flag is false
Latch FROM	-	do not latch FROM frame data from data lines
	enable	latch FROM frame data from data lines at the end of this frame
Latch D1	-	do not latch D1 frame data from data lines
	enable	latch D1 frame data from data lines at the end of this frame
Latch D2	-	do not latch D2 frame data from data lines
	enable	latch D2 frame data from data lines at the end of this frame
Set RFull	-	do not set RFull flag
	enable	set RFull flag at the end of this frame

OBSERVATION 4.2.2.2.1-5:

Since the RFull flag can change asynchronous to the MSIB Internal bus clock it is necessary to synchronize it by latching it on the rising edge of the clock. This latched signal is then input to the state machine.

4.2.2.2.2 Signals

RULE 4.2.2.2.2-1:
Any frame in which BSY is asserted that immediately follows another frame in which BSY is asserted **MUST** be ignored by the module receiver.

RULE 4.2.2.2.2-2:
The module MSIB internal bus receiver **MUST NOT** assert BSY in the TO or D2 frame of a packet.

RULE 4.2.2.2.2-3:
The module MSIB internal bus receiver **MUST NOT** assert BSY in the FROM frame of a packet unless its address matches the to address of the packet.

OBSERVATION 4.2.2.2.2-4:
Note that the conditions set forth in 4.2.1.1 apply here.

4.2.2.2.3 Timing

RULE 4.2.2.2.3-1:
The following parameters as described in figure 4-2 and table 4-3 **MUST** be met by a module's MSIB internal transmitter:

BaHd BaSu ClkBa D8Su DHd DSu

RULE 4.2.2.2.3-2:
The times described in figure 4-2 and table 4-3 **MUST** be met by the module's MSIB internal bus receive section.

4.2.2.3 Module Reset

When a module's MSIB internal interface detects that the MSIB internal RESET line has been asserted it removes itself from the bus by releasing the bus data lines if it was driving them and by releasing its RTS signal if it had it asserted. It is important that this be done quickly in order to insure that it does not send any bad packets when the arbiter starts running, which is shortly after RESET is asserted.

In most cases the module interface will use the RESET signal from the MSIB internal bus to reset the module processor. If the RESET signal is not used to reset the processor then it will be used as an input to the processor such that the module firmware is informed when the RESET signal is asserted or released. This is required in order to meet the protocol requirements described elsewhere in this document.

Since not all mainframes allow a module to assert the RESET signal, when a module attempts to assert RESET it should check to make sure that attempt succeeded. To do this the module attempts to drive the RESET signal low and immediately checks to see whether the signal actually went low. If the signal remained at a logic high level then the mainframe is not capable of accepting a reset signal from a module and the module must immediately cease attempting to drive it low. If the module senses that RESET went low then it was successful in putting the system into reset.

RULE 4.2.2.3-1:
The MSIB internal RESET line **MUST** reset the MSIB internal interface of a module such that the module releases its RTS line within 150 ns after the assertion of RESET.

RULE 4.2.2.3-2:
When attempting to reset a mainframe by pulling the MSIB internal RESET signal low a module **MUST** do so with a series resistance of 100 Ω or a maximum sink current of 20 mA at 2.0 V.

4.2.3 Mainframe

4.2.3.1 Backplane

4.2.3.1.1 CLK

The MSIB internal CLK signal is generated by the mainframe. The mainframe drives the CLK signal with a 6.2 MHz clock while packets are being sent over the bus and holds it low when the bus is idle. The mainframe will start the clock in response to a request to send from either a module or the mainframe translator. The mainframe will keep the clock active for the duration of the packet. If the packet is being sent by a module then the packet is terminated by the assertion of BSY. If the packet is being sent from the mainframe translator then the assertion of BSY will not necessarily terminate the packet. It is therefore necessary for the mainframe translator to signal the mainframe clock generator when a packet must continue with BSY asserted.

RULE 4.2.3.1.1-1:
The mainframe **MUST** activate the CLK signal in response to an RTS signal from either a module or the mainframe translator.

RULE 4.2.3.1.1-2:
The mainframe **MUST** keep the CLK signal active through the frame in which BSY is asserted.

RULE 4.2.3.1.1-3:
The mainframe **MUST** only generate the CLK signal when a packet is in progress or when MSIB internal RESET is asserted.

RULE 4.2.3.1.1-4:
The mainframe **MUST** generate the CLK signal for at least one clock cycle before the RESET signal is released.

RULE 4.2.3.1.1-5:
When there is no packet in progress and RESET is not asserted CLK **MUST** be held at a logic low.

4.2.3.1.2 BSY

RULE 4.2.3.1.2-1:
The mainframe **MUST** assert BSY when no packet is being transmitted.

RULE 4.2.3.1.2-2:
The mainframe **MUST** assert BSY in the D2 frame of a packet if it was not asserted in an earlier frame.

RULE 4.2.3.1.2-3:
The mainframe **MUST** pre-charge the BSY signal during the CLK low time of any frame in which it is not going to assert BSY.

PERMISSION 4.2.3.1.2-4:
The mainframe may elect to not pre-charge the BSY signal if it will be asserting BSY later in the cycle.

RULE 4.2.3.1.2-5:
The mainframe **MUST NOT** pre-charge the BSY signal when the bus is not being clocked.

4.2.3.1.3 ACK

RULE 4.2.3.1.3-1:
The mainframe **MUST** pre-charge the ACK signal during the CLK low time of each active frame.

4.2.3.1.4 RTS

RULE 4.2.3.1.4-1:
The mainframe **MUST** passively pull high (false) any RTS line which is not being driven because a module has not been installed.

4.2.3.1.5 Timing

RULE 4.2.3.1.5-1:
The following parameters as described in figure 4-2 and table 4-3 **MUST** be met by a module's MSIB internal transmitter:

ClkCyc ClkH ClkL ClkPc ClkSkew PcHd

4.2.3.2 Arbiter

The function of the MSIB internal bus arbiter is to arbitrate the use of the MSIB internal bus between various modules and the mainframe translator.

4.2.3.2.1 Arbitration

The MSIB internal arbitration algorithm is designed to give all modules equal access to the bus. It is also designed to allow packets from the mainframe translator to be processed quickly enough that the external bus does not become congested. The algorithm can be described as follows:

1. The bus is allocated on a packet by packet basis, regardless of the length of the packets. These packets can also be thought of as time slots, although they actually vary in length.
2. The slots are divided 50% for the mainframe translator and 50% for the modules.
3. The module slots are divided equally between the modules.
4. The granting of slots to modules is done on a round-robin basis. After a module has used a slot it is assigned the lowest priority. The next module in sequence takes on the highest priority, with the remainder of the modules taking on successively lower priorities.
5. Any component that is not requesting a slot but would have been granted one if it was requesting one gives up its position. The arbitration proceeds as though the module had used its slot.

RULE 4.2.3.2.1-1:
For each packet on the bus the arbiter **MUST** grant a time slot to only one component.

RULE 4.2.3.2.1-2:
The arbiter **MUST NOT** assert CTS to a module that is not asserting RTS.

RULE 4.2.3.2.1-3:
The arbiter **MUST** grant half the available time slots to the mainframe translator if it requests them.

RULE 4.2.3.2.1-4:
The arbiter **MUST** divide the time slots not used by the mainframe translator equally between those modules requesting use of the bus..

RULE 4.2.3.2.1-5:
The arbiter **MUST** ignore all module RTS signals when the MSIB internal RESET signal is asserted.

4.2.3.2.2 Signals

OBSERVATION 4.2.3.2.2-1:
Note that the conditions set forth in 4.2.1.1 apply here.

4.2.3.2.3 Timing

RULE 4.2.3.2.3-1:
The following parameters as described in figure 4-2 and table 4-3 **MUST** be met by a module's MSIB internal transmitter:

BaHd BaSu ClkBa ClkCtsH ClkCtsL

4.2.3.3 Translator

The purpose of the mainframe translator is to act as a transparent interface between the MSIB internal bus and modules not on that bus. It does this by transferring packets between the MSIB internal bus and the MSIB external bus. Packets from the MSIB internal bus that need to be sent to other mainframes are received by the translator and transferred to the MSIB external bus interface. Packets coming from other mainframes are transferred from the MSIB external bus interface to the MSIB internal bus.

Since the MSIB external bus is a loop, a packet sent from a mainframe will be passed from one mainframe to the next until it returns to the mainframe from which it was sent. That mainframe will not forward the packet, thus breaking the loop.

A packet coming in from the MSIB external interface is transferred to the MSIB internal bus. If the sender of the packet is not in this mainframe then the packet will be transferred back to the external interface to be passed on to the next mainframe in the loop. The EA and NA bits of the packet will be modified as appropriate based on the presence or absence of the destination module in this mainframe.

4.2.3.3.1 Outgoing Packets

An outgoing packet is any packet that is from a module in a mainframe to a module not in that mainframe. If the mainframe translator detects the need to forward a packet but does not have room to receive the packet then it must assert BSY in the D1 frame. The sender of the packet will use this as a signal to retransmit the packet.

Note that the mainframe translator must take all packets not acknowledged in the mainframe even if it is able to recognize that there is no module outside the mainframe who's address matches the TO address of the packet.

The mainframe translator takes a packet off the bus by capturing the values of all frames of the packet. The packet is then transmitted to other mainframes in which the receiver might be contained.

Once the packet has been delivered to the receiving module or it has been determined that cannot be delivered, the packet is returned to the sending module by way of the internal bus. When the packet is returned to the module the EA and NA bits of the packet indicate whether or not a receiving module for the packet was found and whether or not the receiving module was able to accept the packet.

When the packet is returned to the internal bus the sending module acknowledges recognition of its FROM address by asserting ACK in the D1 frame. The mainframe translator may use this signal as the indication that the packet has been returned to its sender.

4.2.3.3.1.1 Mainframe Translator Receive Algorithm

The mainframe translator receive algorithm is described in figure 4-6. The algorithm description uses the state machine notation defined in section 1.4.3. This description is not intended as an implementation of the algorithm. An actual implementation would quite likely differ from the state machine shown here. All state transitions occur on the high to low transition of CLK. A mainframe translator receiver never drives the internal bus data lines.

On reset the mainframe translator state machine enters state A.

A: The mainframe stays in state A until the end of the first frame of a packet (the TO frame). If at the end of the TO frame the mainframe's receive buffer is full the mainframe will go either to state G or to state H where it may abort the packet. It will go to state G if the packet is being sent by the mainframe and to state H if it is being sent by a module. If the mainframe's input buffer is not full it will latch the TO frame data of the packet and go to either state B or to state E (B if module, E if mainframe).

B: The mainframe will stay in state B until the end of the FROM frame of the packet. If at the end of the FROM frame either the ACK or BSY signal is set, the mainframe will quit receiving the packet and return to state A. The ACK bit will be set if the destination module is contained in this mainframe, in which case there is no need to send the packet over the external bus. The BSY bit set indicates that the packet was aborted for some reason. If neither of these bits is set the mainframe will latch the FROM frame data and continue to state C.

C: The mainframe will stay in state C until the end of the D1 frame of the packet. If at the end of the FROM frame either the ACK or BSY signal is set the mainframe will quit receiving the packet and return to state A. As in the FROM frame, BSY asserted at the end of the D1 frame indicates that the packet has been aborted. The ACK bit set indicates that the packet is being removed from the bus and therefore should not be passed to the external bus. If neither of these bits is set the mainframe will latch the D1 frame data and continue to state D.

D: The mainframe will stay in state D until the end of the D2 frame. At the end of the D2 frame the mainframe will latch the D2 frame data and set a flag (Rfull) indicating a packet has been received. This packet will then be sent on to the external bus. The mainframe will then return to state A to await the next packet.

E: The mainframe will enter state E in the FROM frame if the packet being sent is being sent by the mainframe. If at the end of the FROM frame neither the BSY nor ACK signal is asserted, the mainframe will latch the FROM frame data and go to state C. This will occur when the receiver of the packet is not in this mainframe. If at the end of the FROM frame either the BSY or ACK signal is asserted the mainframe will latch the FROM frame and continue to state F. If the ACK signal is asserted the mainframe will set the EA bit of the packet, indicating that the receiver of the packet was found. If the BSY signal is asserted the mainframe will set the NA bit of the packet indicating that the receiver was unable to accept the packet. Note that the mainframe will not return to state A even if the BSY signal is asserted. In this case the mainframe will continue to clock the remainder of the packet with the BSY signal asserted for each frame. This allows the transmit portion of the mainframe translator to pass the remainder of the packet to the receive portion so it can be sent on to the next mainframe in the external loop.

F: The mainframe remains in state F until the end of the D1 frame. At the end of the D1 frame the mainframe checks the ACK line. If ACK is asserted at the end of the D1 frame then the sender of the packet is in this mainframe and the packet should not continue on the external bus. In this case the mainframe returns to state A to wait for the next packet. If ACK is clear at the end of the D1 frame then the mainframe will latch the D1 data and go to state D. If BSY is asserted the mainframe will set the NA bit of the packet. Again, this is an indication that the receiver was unable to accept the packet. Note once again that the mainframe will not return to state A even if BSY is asserted.

G: The mainframe enters state G in the FROM frame of a packet if the receive buffer is full and the packet is being sent by the mainframe. If at the end of the FROM frame the BSY signal is asserted the mainframe will return to state A to await the next packet. If the BSY signal is not asserted at the end of the FROM frame then the mainframe will assert BSY to abort the packet and continue to state J.

H: The mainframe enters state H in the FROM frame of a packet if the receive buffer is full and the packet is being sent by a module. The mainframe will return to state A at the end of the FROM frame if either the BSY or ACK signal is asserted. If BSY is asserted then the packet has terminated early and there is no need for the mainframe to terminate the packet. If ACK is asserted then the receiver of the packet is in the same mainframe and therefore would have been ignored by the mainframe receiver anyway. If neither BSY nor ACK is asserted then the mainframe aborts the packet by asserting BSY and continuing to state J.

J: The mainframe enters state J in the D1 frame when it has been determined that the packet must be aborted. The mainframe accomplishes this by asserting BSY in this (D1) frame. At the end of the D1 frame the mainframe returns to state A to await the next packet.

RULE 4.2.3.3.1.1-1:

A mainframe translator receiver **MUST** implement all states of the mainframe translator receive algorithm (figure 4-6).

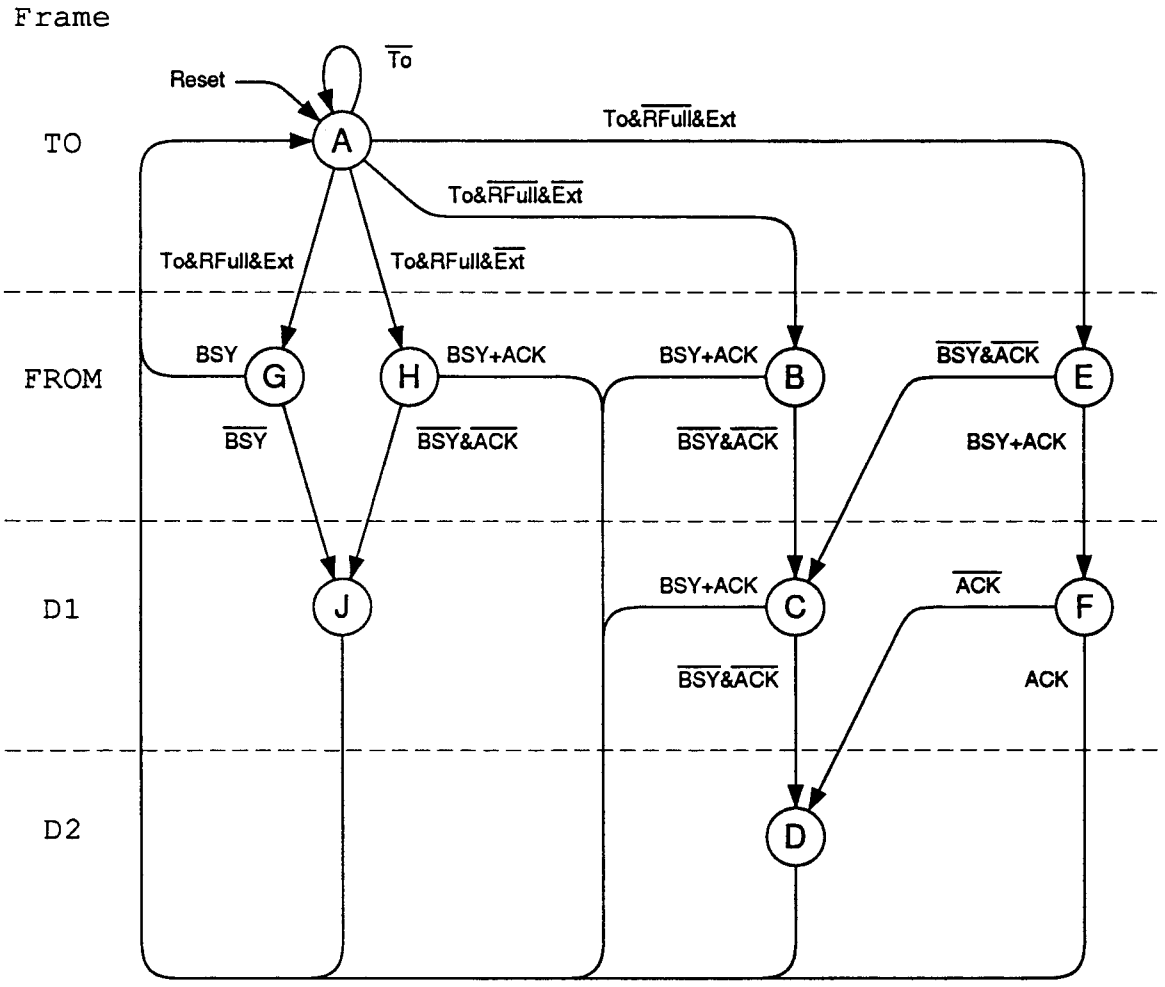


Figure 4-6. Mainframe Translator Receive Algorithm

TABLE 4-8. Mainframe Translator Receive Algorithm Notation

States:

A	Idle or TO frame
B	FROM frame, receiver not full, packet from module
C	D1 frame
D	D2 frame
E	FROM frame, receiver not full, packet from external
F	D1 frame, external
G	Receiver full, from external
H	Receiver full, from module
J	Aborting packet

Conditions:

ACK	MSIB internal bus ACK signal
BSY	MSIB internal bus BSY signal
Ext	Translator transmitter is active (not in state A)
Reset	MSIB internal bus RESET signal
TO	TO frame - frame with BSY false following frame with BSY true
RFull	State of RFull flag latched on rising edge of CLK (see observation 4.2.3.3.1.1-2)

Outputs:

State	BSY	Latch TO	Latch FROM	Latch D1	Latch D2	Set EA	Set NA	Set RFull
A	-	if not RFull	-	-	-	-	-	-
B	-	-	enable	-	-	-	-	-
C	-	-	-	enable	-	-	-	-
D	-	-	-	-	enable	-	-	enable
E	-	-	enable	-	-	if ACK	if BSY	-
F	-	-	-	enable	-	-	if BSY	-
G	-	-	-	-	-	-	-	-
H	-	-	-	-	-	-	-	-
J	assert	-	-	-	-	-	-	-

BSY	-	do not assert BSY
	assert	assert BSY during the CLK low time of this frame
Latch TO	-	do not latch TO frame data from data lines
	if not RFull	Latch TO frame from the data lines at the end of this frame if the latched value of the RFull flag is false
Latch FROM	-	do not latch FROM frame data from data lines
	enable	latch FROM frame data from data lines at the end of this frame
Latch D1	-	do not latch D1 frame data from data lines
	enable	latch D1 frame data from data lines at the end of this frame
Latch D2	-	do not latch D2 frame data from data lines
	enable	latch D2 frame data from data lines at the end of this frame
Set EA	-	do not change the setting of the EA field of the packet
	if ACK	set the EA field of the packet true
Set NA	-	do not change the setting of the NA field of the packet
	if BSY	set the NA field of the packet true
Set RFull	-	do not set RFull flag
	enable	set RFull flag at the end of this frame

OBSERVATION 4.2.3.3.1.1-2:
Since the RFull flag can change asynchronous to the MSIB Internal bus clock it is necessary to synchronize it by latching it on the rising edge of the clock. This latched signal is then input to the state machine.

4.2.3.3.1.2 Signals

OBSERVATION 4.2.3.3.1.2-1:
Note that the conditions set forth in 4.2.1.1 apply here.

4.2.3.3.1.3 Timing

RULE 4.2.3.3.1.3-1:
The following parameters as described in figure 4-2 and table 4-3 **MUST** be met by a module's MSIB internal transmitter:

BaHd BaSu ClkBa D8Su DHd DSu

4.2.3.3.2 Incoming Packets
Incoming packets are packets from modules outside this mainframe that have been delivered to the mainframe translator for attempted delivery to modules in this mainframe. The mainframe translator attempts to deliver these packets by placing them on the MSIB internal bus. When placing a packet on the bus the mainframe translator must watch the BSY and ACK lines to determine whether a receiver for the packet is in this mainframe and (if it is) whether or not the receiver is busy. This information is then returned to the module that sent the packet.

Note that the assertion of BSY by the receiving module would normally terminate the packet. In this case if the receiver is busy the remainder of the packet still needs to go over the bus. To this end the mainframe translator communicates with the mainframe and the arbiter to insure that the clock remains active and that no other modules are granted a time slot on the bus until this packet is complete, in spite of the fact that BSY is asserted during the last two or three frames of the packet.

RULE 4.2.3.3.2-1:
The mainframe translator **MUST** transfer any incoming packet to the MSIB internal bus.

4.2.3.3.2.1 Mainframe Translator Transmit Algorithm
The mainframe transmitter algorithm is described in figure 4-7. The algorithm description is in the form of a state machine as defined in section 1.4.3. This description is not intended as an implementation of the algorithm. An actual implementation would quite likely differ from the state machine shown here. All state transitions occur on the high to low transition of CLK. On RESET the mainframe translator transmit section enters state A.

A: The mainframe remains in state A until it receives a CTS signal during the first frame of a packet. While in state A it will assert RTS if it has a packet to send and CTS is not asserted. When CTS is asserted the module will asynchronously release RTS and drive its TO frame data onto the data lines. If the mainframe receives CTS during the first frame of a packet and it has a

packet to send, then it continues to state B and sets a flag (Ext) indicating that the current packet is being sent by the mainframe translator. If the mainframe receives CTS during the first frame of a packet and it has no packet to send, then it goes to state G to abort the packet.

B: The mainframe remains in state B for the duration of the FROM frame. While in state B the mainframe drives the data lines with FROM frame data of the packet it is sending. At the end of the FROM frame the mainframe checks the signals BSY, ACK, and RFull (mainframe translator receiver full). If BSY is asserted and the mainframe translator receiver is full (RFull) then the packet has been aborted and the mainframe returns to state A. If BSY is asserted but the translator receiver is not full then the packet will continue to completion. Since BSY was asserted in the FROM frame and the packet is going to continue anyway, it is necessary for the mainframe to also assert BSY in the D1 frame so as not to indicate the start of a new packet (since the release of BSY signals the start of a packet). The mainframe continues to state C.

If BSY was not asserted in the FROM frame but ACK was asserted, then the destination module is in this mainframe and is able to receive the packet. The mainframe proceeds to state E. If neither BSY nor ACK were asserted then the destination module is not in this mainframe and the mainframe goes to state F.

C: The mainframe remains in state C for the duration of the D1 frame. While in state C the mainframe drives the packet D1 frame data to the data lines and also asserts BSY. BSY must be asserted in this frame since it was asserted in an earlier frame. At the end of the D1 frame the mainframe continues to state D.

D: The mainframe remains in state D for the duration of the D2 frame. While in state D the mainframe drives the packet D2 frame data to the data lines. At the end of the D2 frame the mainframe returns to state A. At this time it clears the Trdy flag to indicate that the packet has been sent.

E: The mainframe enters state E in the D1 frame when the destination module is in this mainframe and is able to accept the packet. While in state E the mainframe drives the data lines with the D1 frame data from the packet. If the mainframe receive buffer is full and ACK is not asserted in the D1 frame the mainframe will return to state A. Since ACK is not asserted in D1 the sender of the packet is not in this mainframe, and therefore the mainframe receiver must send the packet to the next mainframe. Note that if this is the case the BSY signal will be asserted in the D1 by the mainframe receiver.

If ACK and BSY are both asserted at the end of the D1 frame the mainframe will clear the Trdy flag to indicate that the packet has been sent and return to state A. This happens when the sender of the packet is in this mainframe. In this case the mainframe receiver doesn't have to pass the packet on so it doesn't matter whether or not the mainframe receiver can accept the packet. The assertion of BSY in this case terminates the packet.

The assertion of ACK without BSY is also an indication that the sender of the packet is in this mainframe. In this case, however, the packet is not terminated in the D1 frame. The mainframe proceeds to state D where it will send the D2 frame.

If ACK is not asserted and the mainframe receiver can accept the packet (RFull false) then the packet progresses to completion so the mainframe receiver can pass it on to the next mainframe. The mainframe proceeds to state D.

F: The mainframe enters state F in the D1 frame if neither BSY nor ACK are asserted in the FROM frame, indicating that the destination module is not in this mainframe. While in state F the mainframe drives the D1 frame packet data on the data lines. If at the end of the D1 frame BSY is asserted but ACK is not then the packet is being aborted and the mainframe returns to state A. This will typically occur when the mainframe receive buffer is full. If BSY and ACK are both asserted then the sender of the packet is in this mainframe and the packet will not be sent to the next mainframe. The mainframe clears the Trdy line to indicate the packet has been sent and

returns to state A. If the BSY signal is asserted then the packet will proceed to completion. The mainframe goes to state D to send the D2 frame data.

G: State G is entered when the mainframe received a CTS but has no packet to send. The mainframe remains in state G for the duration of the FROM frame but does not drive the data bus. If BSY is asserted at the end of the FROM frame then the mainframe returns to state A. Otherwise the mainframe continues to state H where it will assert BSY to terminate the packet.

H: In state H the mainframe asserts the BSY signal but does not drive the data lines. The assertion of BSY in the D1 frame will terminate the packet.

RULE 4.2.3.3.2.1-1:

A mainframe translator transmitter **MUST** implement states A through F of the mainframe translator transmit algorithm (figure 4-7).

RECOMMENDATION 4.2.3.3.2.1-2:

A mainframe translator transmitter should implement states G and H of the mainframe translator transmitter algorithm (figure 4-7). These states will normally not be executed, but they prevent an errant CTS from generating an invalid MSIB packet.

PERMISSION 4.2.3.3.2.1-3:

A mainframe translator transmitter may assert RTS for the duration of a packet if it has another packet to send that can be sent immediately following the current one. In this case RTS remains asserted when CTS becomes true in state A.

OBSERVATION 4.2.3.3.2.1-4:

There is no way for a mainframe translator transmitter to abort a transmission.

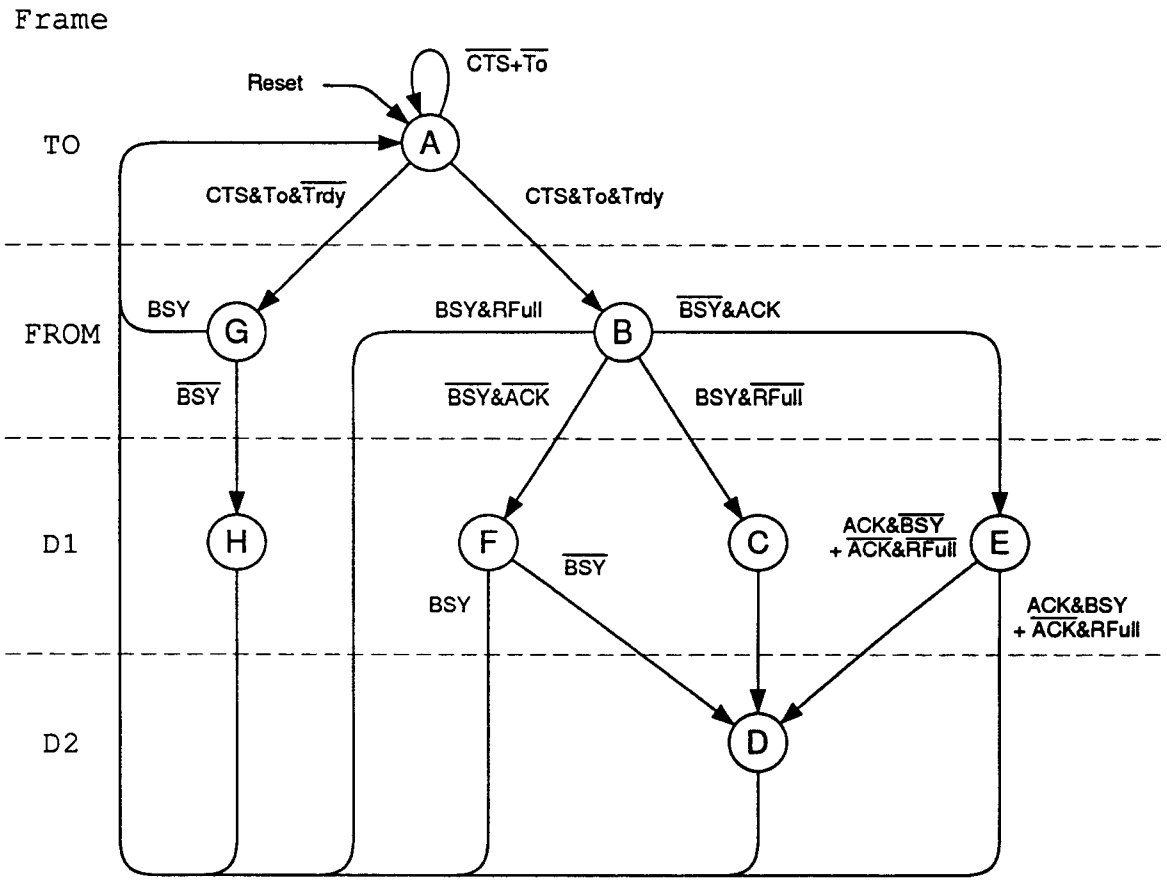


Figure 4-7. Mainframe Translator Transmit Algorithm

TABLE 4-9. Mainframe Translator Transmit Algorithm Notation

States:

A	Idle or TO frame
B	Sending FROM frame of packet
C	Sending D1 frame, receiving module busy
D	Sending D2 frame
E	Sending D1 frame, receiving module present and not busy
F	Sending D2 frame, receiving module not present
G	Errant CTS from Arbiter
H	Terminate packet in D1

Conditions:

ACK	MSIB internal bus ACK signal
BSY	MSIB internal bus BSY signal
CLK	High to Low transition of MSIB internal bus CLK signal
CTS	Clear TO Send signal from Arbiter
Reset	MSIB internal bus RESET signal
TO	TO frame - frame with BSY false following frame with BSY true
RFull	State of RFull flag latched on rising edge of CLK
Trdy	state of Trdy flag latched on rising edge of CLK (see observation 4.2.3.3.2.1-5)

Outputs:

State	BSY	Drive TO	Drive FROM	Drive D1	Drive D2	Clear TRDy	RTS
A	-	if CTS	-	-	-	-	if ready
B	-	-	drive	-	-	-	-
C	assert	-	-	drive	-	-	-
D	-	-	-	-	drive	enable	-
E	-	-	-	drive	-	if done	-
F	-	-	-	drive	-	if done	-
G	-	-	-	-	-	-	-
H	assert	-	-	-	-	-	-

BSY	-	do not assert BSY
	assert	assert BSY during the CLK low time of this frame
Drive TO	-	do not drive data lines with TO frame data
	if CTS	drive data lines with TO frame data while CTS is asserted
Drive FROM	-	don
	drive	drive data lines with FROM frame data
Drive D1	-	do not drive data lines with D1 frame data
	drive	drive data lines with D1 frame data
Drive D2	-	do not drive data lines with D2 frame data
	drive	drive data lines with D2 frame data
Clear Trdy	-	do not clear Trdy flag
	enable	clear Trdy flag at the end of this frame
	if done	clear Trdy flag at the end of this frame if BSY is asserted and ACK is asserted
RTS	-	do not assert RTS
	if ready	assert RTS while the Trdy flag is and and CTS is not asserted

OBSERVATION 4.2.3.3.2.1-5:
Since the Trdy flag can change asynchronous to the MSIB Internal bus clock it is necessary to synchronize it by latching it on the rising edge of the clock. This latched signal is then input to the state machine.

4.2.3.3.2.2 Signals

OBSERVATION 4.2.3.3.2.2-1:
Note that the conditions set forth in 4.2.1.1 apply here.

4.2.3.3.2.3 Timing

RULE 4.2.3.3.2.3-1:
The times described in figure 4-2 and table 4-3 **MUST** be met by the mainframe translator's MSIB internal bus receive section.

4.2.3.4 Mainframe Reset
The MSIB internal bus RESET signal is used to indicate or to initiate a system reset. When this signal is asserted it is an indication to all modules that the system is in reset. The signal may be asserted by either the mainframe translator or by a module.

The mainframe will assert MSIB internal bus RESET either when it is powering up or down (the power supplied to the modules is not within the specified range) or when its mainframe translator detects a reset signal initiated from outside this mainframe(e.g. from another mainframe). A module will assert RESET in order to reset the system.

RULE 4.2.3.4-1:
A mainframe **MUST** delay the negation of RESET until at least 100 ms after the distributed power comes within its specified range.

RECOMMENDATION 4.2.3.4-2:
A mainframe should assert RESET as long as the distributed power is outside the specified range.

OBSERVATION 4.2.3.4-3:
A mainframe might not assert RESET if the distributed power falls outside the specified range.

OBSERVATION 4.2.3.4-4:
If the distributed power leaves then reenters its specified range RESET will be asserted as described above.

RULE 4.2.3.4-5:
If a mainframe is not pulling the MSIB internal RESET signal low it **MUST** passively pull it to a logic high level with the equivalent of 5 KΩ ± 5% to 5 V ± 5%.

RULE 4.2.3.4-6:
A mainframe that does not provide for module initiated reset **MUST** drive the RESET line high with a minimum of 60 mA to a minimum of 2.0 V.

4.2.3.5 Bus Characteristics

RULE 4.2.3.5-1:
All MSIB internal bus signal lines **MUST** have a capacitance of less than 100 pF at 1 kHz with respect to ground.

RULE 4.2.3.5-2:
All MSIB internal bus signal lines **MUST** have a line impedance of between 40 and 70 Ω.

RECOMMENDATION 4.2.3.5-3:
All MSIB internal bus signal lines should have an electrical length (propagation delay) of less than 4 ns. This is the time it takes for a signal to propagate from one end of the bus to the other.

RULE 4.2.3.5-4:
All MSIB internal bus signals **MUST** be terminated in the mainframe by the equivalent of 180 Ω ± 4 Ω to 2.7 V ± 0.15 V.

OBSERVATION 4.2.3.5-5:
180 Ω to 2.7 V is the equivalent of a resistive divider of 330 Ω TO 5 V and 390 Ω to 0 V.

4.3 MSIB External Bus

4.3.1 Overview

The MSIB external bus is a bus that transmits packets between mainframes. The MSIB external bus interface transfers packets between the MSIB external bus and the mainframe translator. The mainframe translator then transfers packets between the MSIB external bus interface and the MSIB internal bus.

The MSIB external bus is organized as a loop with a cable connecting the "Out" connector of each mainframe to the "In" connector of the next. Packets flow unidirectionally around this loop. There is no limit to the number of mainframes that can be connected together.

The MSIB external bus interface takes packets that the mainframe translator has determined need to go to other mainframes and transfers them to the next mainframe in the loop. It also takes packets from the previous mainframe in the loop and transfers them to the mainframe translator.

The MSIB mainframe translator has a fifo on its input side that can hold at least as many packets as there can be modules in the mainframe. This insures that each module in the mainframe can have one packet circulating around the external bus without leading to a possible deadlock condition.

If the either the "In" or the "Out" connector does not have a cable connected to it then the mainframe will internally route packets back to itself as though there was a cable connecting the "In" connector to the "Out" connector. This is necessary because the mainframe translator will transfer to the MSIB external interface all packets that it feels need to be sent to other mainframes. The MSIB external

interface will then need to return these packets to the mainframe translator such that they can be returned to their originating module.

RULE 4.3.1-1:
An MSIB external interface **MUST** have a fifo that can hold at least as many packets as there can be modules in the mainframe in the data path from the MSIB external bus to the mainframe translator.

RULE 4.3.1-2:
An MSIB mainframe translator with no cables connected **MUST** function as though there was a cable connecting it to itself.

OBSERVATION 4.3.1-3:
The system will fail if this rule is not followed and no cables are connected and a module in the mainframe attempts to send data to a module not in this mainframe.

4.3.1.1 Frames
Packets on the MSIB external bus are organized into frames in much the same manner as they are on the MSIB internal bus. The frames on the MSIB external bus, however, have an additional pair of signals to uniquely identify the frames. The frames are defined as follows:

TABLE 4-10. Frame Definitions

Frame	D0-7	D8	FR1	FR0
FROM	FROM ADDRESS	EA	0	1
TO	TO ADDRESS	B/W	0	0
D1	DATA 1	NA	1	0
D2	DATA 2	CMD	1	1

4.3.1.2 Signals
The MSIB external signals are defined as follows:

TABLE 4-11. External Signal Definitions

Name	Description	In	Out	Type	Assertion Level
DAV	Data available	Rec	Drv	Differential	active low
DAC	Acknowledge	Drv	Rec	Differential	active low
D8,D7/0	Data	Rec	Drv	Differential	positive logic
FR0-1	Frame ID	Rec	Drv	Differential	positive logic
RESET	Reset	Rec	Drv	Single Ended	active low
SRDY	Source ready	Rec	Drv	Single Ended	active high
DRDY	Dest. ready	Drv	Rec	Single Ended	active high
CABLE	Cable present	Rec	Rec	Single Ended	active low

The "In" column indicates whether the signal is driven or received on the "In" connector. The "Out" column indicates whether the signal is driven or received on the "out" connector.

4.3.1.2.1 DAV and DAC

These signals are used together to handshake the data from the sender to the receiver. The DAV signal is driven by the sender and indicates the presence of a frame of data on the data lines. The DAC signal is driven by the receiver and is used to complete the handshake.

4.3.1.2.2 D8 Through D0

These signals carry the 9 data bits of a frame.

4.3.1.2.3 FR0 and FR1

These lines indicate which frame of the packet is present on the data lines.

4.3.1.2.4 RESET, SRDY, DRDY

These signals are used to communicate the reset status between mainframes. The goal is that a reset signal generated in one mainframe should cause all the other mainframes in the loop to go into reset.

The signals SRDY (source ready) and DRDY (destination ready) are used to signal the status of adjacent mainframes. These are active high signals that indicate when the mainframes have power applied and are ready to run. These lines are pulled low by the mainframe when the mainframe is not ready, including when power is not applied.

RESET is the signal used to communicate reset information between mainframes in a system. This is an active low signal by which a mainframe indicates to the next mainframe in a loop that a reset condition is present. The mainframe receiving the RESET signal will conditionally pass the signal on to the next mainframe in the loop. This continues until all mainframes in a loop have entered reset. The reset algorithm is designed such that the mainframe originating the signal is also responsible for removing it.

RULE 4.3.1.2.4-1:
The SRDY and DRDY signals driven by a mainframe **MUST** be held low until the MSIB mainframe translator is ready to handle MSIB communications.

RULE 4.3.1.2.4-2:
The SRDY, DRDY, and RESET signals out of a mainframe **MUST** be held low when there is no power applied to the mainframe.

RULE 4.3.1.2.4-3:
The RESET, SRDY, and DRDY signals **MUST** be driven according to the reset algorithm described in the section 4.3.5.

RULE 4.3.1.2.4-4:
If the DRDY signal into a mainframe is low (false) then the mainframe **MUST NOT** attempt to send packet frames to the next mainframe in the loop.

RULE 4.3.1.2.4-5:
If the SRDY signal into a mainframe is low (false) then the mainframe **MUST NOT** receive frames from the previous mainframe in the loop. In other words, it **MUST** ignore the handshake lines from the previous mainframe.

4.3.1.2.5 CABLE
The CABLE signal is used to indicate that a cable is connected to either the "In" or "Out" connector. Note that this signal is an input on both of these connectors. This signal is passively pulled high by the mainframe. When a cable is connected it pulls this signal to ground. This is accomplished by connecting the CABLE signal in each connector to a ground pin in that same connector.

RECOMMENDATION 4.3.1.2.5-1:
The CABLE signal of each connector should be passively pulled high such that a high level is detected if the signal has no connections to it and a low level is detected if it is connected to ground.

4.3.1.3 Frame Transmission
Packets are transmitted from one mainframe to another one frame at a time.

RECOMMENDATION 4.3.1.3-1:
The MSIB mainframe translator **MUST** transmit packets in the order TO, FROM, D1, D2.

RECOMMENDATION 4.3.1.3-2:
An MSIB mainframe translator receiver should accept the TO, FROM, and D1 frames in any order.

RULE 4.3.1.3-3:
An MSIB mainframe translator receiver **MUST** accept the D2 frame as the last frame of a packet.

OBSERVATION 4.3.1.3-4:

Receipt of a D2 frame is the indication that the packet is complete.

RECOMMENDATION 4.3.1.3-5:

An MSIB mainframe translator receiver should construct packets using the last transmitted value of each frame. In other words, if a frame is omitted from a packet the receiver should use the data that was contained in that frame the last time the frame was sent.

4.3.1.3.1 Frame Handshake

The transfer of each frame is accomplished by a handshake between the transmitter and the receiver. This handshake insures reliable transmission of the data regardless of the length of the cable through which the data sent. As longer cables are used the handshake mechanism slows the data transfer to make up for the fact that the signal's integrity is degraded. This handshake is shown in figure 4-8.

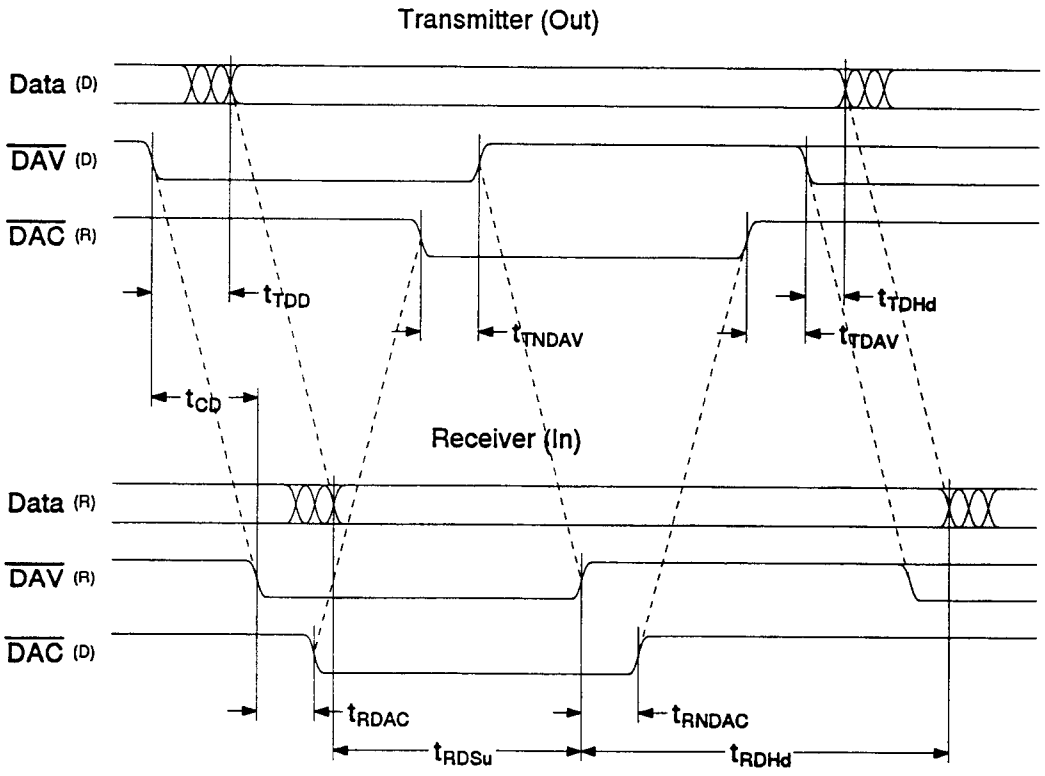


Figure 4-8. Frame Handshake

TABLE 4-12. Frame Handshake Time Symbols

Symbol	Description
tCD	Cable delay - Time for a signal to traverse the cable
tRDAC	Receiver delay from DAV asserted to DAC asserted
tRDSu	Receiver data setup to DAV release
tRDHd	Receiver data hold after DAV release
tRNDAC	Receiver delay from DAV released to DAC released
tTDAV	Transmitter delay from DAC released to DAV asserted
tTDD	Transmitter delay from DAV asserted to Data valid
tTDHd	Transmitter data hold time after DAV asserted
tTNDAV	Transmitter delay from DAC asserted to DAC released

The handshake operates as follows:

1. The sending mainframe waits for the receiving mainframe to release DAC before starting the transfer.
2. The sending mainframe drives the data lines with the frame data and asserts DAV.
3. When the receiving mainframe detects the assertion of DAV and it has input buffer space available it responds by asserting DAC.
4. The sending mainframe responds to the assertion of DAC by releasing DAV.
5. The receiving mainframe uses the release of DAV to latch the frame into its input buffer. It then releases DAC.
6. When the sending mainframe detects the release of DAC it can then drive the data lines with the data from the next frame and assert DAV.

4.3.1.3.2 Frame Handshake Timing

In order for the receiver to properly receive the data it is necessary for the data arriving to meet setup and hold times relative to the signal edge on which the data is latched. Let's deal first with the setup time. The setup time for data arriving at the receiver is given by the following formula (see figure 4-8):

$$t_{RDSu} = (t_{CD} + t_{RDAC} + t_{CD} + t_{TNDAV} + t_{CD}) - (t_{TDD} + t_{CD})$$

The analysis of these timings falls into two categories, short cables and long cables. First let's deal with short cables.

4.3.1.3.2.1 Short Cables

For short cables it can be assumed that the delay contributed by the cables is zero. In this case the setup time for data arriving at the receiver is given by the following formula:

$$t_{RDSu} = (t_{RDAC} + t_{TNDAV}) - (t_{TDD})$$

In order that data be received properly it is necessary that the setup time of data arriving at the receiver be greater than the setup time that the receiver requires. We can therefore rewrite the above equation into an inequality that must be satisfied in order that data be transferred properly:

$$t_{RDSu}(max) < t_{RDAC}(min) + t_{TNDAV}(min) - t_{TDD}(max)$$

In order to have a system in which any transmitter will work with any receiver it is necessary to set up rules for both the transmitter and the receiver that when followed insure that they will work together. All variables contained in a rule must represent features of the component to which the rule applies. For example, a rule that applies to the transmitter must only include variables that are under the control of the transmitter. If it includes variables under control of the receiver then the transmitter cannot be guaranteed to work with all receivers. To do this we first rearrange the inequality to place transmitter variables on one side and receiver variables on the other side.

$$t_{RDSu}(max) - t_{RDAC}(min) < t_{TNDAV}(min) - t_{TDD}(max)$$

This inequality cannot be used as a rule because it contains variables from both components. To solve this we break the inequality into two inequalities where each inequality has only variables from one component.

$$t_{RDSu}(max) - t_{RDAC}(min) < 0\ ns < t_{TNDAV}(min) - t_{TDD}(max)$$

These inequalities can then be used to generate the rules at the end of this section.

The data hold formula is very similar to the data setup formula:

$$t_{RDHd} = t_{RNDAC} + t_{TDAV} + t_{TDHd}$$

which yields the inequality:

$$t_{RDHd}(max) < t_{RNDAC}(min) + t_{TDAV}(min) + t_{TDHd}(min)$$

and is then broken into two inequalities from which rules can be derived:

$$t_{RDHd}(max) - t_{RNDAC}(min) < 15\ ns < t_{TDAV}(min) + t_{TDHd}(min)$$

RULE 4.3.1.3.2.1-1:
The transmitter setup time $t_{TNDAV}(min) - t_{TDD}(max)$ **MUST** be greater than 0 ns.

RULE 4.3.1.3.2.1-2:
The receiver setup time $t_{RDSu}(max) - t_{RDAC}(min)$ **MUST** be less than 0 ns.

RULE 4.3.1.3.2.1-3:
The transmitter hold time $t_{TDAV}(min) + t_{TDHd}(min)$ **MUST** be greater than 15 ns.

RULE 4.3.1.3.2.1-4:
The receiver hold time $t_{RDHd}(max) - t_{RNDAC}(min)$ **MUST** be less than 15 ns.

4.3.1.3.2.2 Long Cables
There are three effects that cables have on the signals that we need to consider. The first affect is delay. Signals out of a cable will be delayed from the signals going in by an amount proportional to the length of the cable. The affect this has is to delay the data and each step of the handshake. This results in the setup and hold times for data arriving at the receiver each being increased by twice the cable delay time.

Signals arriving at the end of a cable may not all be delayed by the same amount. This results in a change in the relative timing of signals arriving at the receiver from what they were at the transmitter.

This delay and resulting timing change will be a small fraction of the cable delay time.

The fact that the relative timing of signals arriving at the receiver can change means that the time between data and the clocking signal edge could change, thereby affecting the data setup/hold times. The setup and hold times, however, have been increased by twice the total cable delay time. Since the skew is a small fraction of the cable delay time the setup and hold times will remain well within the limits.

The final factor to consider is that signals arriving at the receiver will not have the clean edges they had when they were sent. The line receivers will turn the signals back into clean logic levels. However, in the process there may be additional skew introduced to the signals. Since the degree to which the signal edges are degraded is roughly proportional to the length of the cable, the additional skew will also be roughly proportional to the length of the cable and therefore should be taken care of by the increased setup and hold times. Therefore, the rules stated in section 4.3.1.3.2.1 will also hold for long cables.

4.3.1.3.2.3 Pulse Width Limits

If a transmitter or receiver has very fast line drivers/receivers it is possible that the handshake will proceed at such a rate that minimum pulse width or maximum frequency limits are exceeded. In such a situation it is permissible for a transmitter or receiver to delay its part of the handshake to insure that such limits are not exceeded. When evaluating a design to determine if such limits might be exceeded it should be assumed there are no delays contributed outside the design being evaluated (e.g. when evaluating a transmitter it should be assumed that cable and receiver delays are zero).

PERMISSION 4.3.1.3.2.3-1:

A transmitter may extend DAV high and/or DAV low times in order to meet its pulse width and/or frequency limits.

PERMISSION 4.3.1.3.2.3-2:

A receiver may extend DAC high and/or DAC low times in order to meet its pulse width and/or frequency limits.

RECOMMENDATION 4.3.1.3.2.3-3:

All delays should be kept as short as possible to maximize performance.

4.3.2 Transceivers

4.3.2.1 Differential Transceivers

RULE 4.3.2.1-1:

A differential transmitter **MUST NOT** exceed a maximum low level of .5 V and **MUST** exceed a minimum high level of 2.5 V.

RULE 4.3.2.1-2:
A 50 Ω resistance **MUST** be put in series with each of the differential lines of a transmitter.

RULE 4.3.2.1-3:
A differential receiver **MUST** determine a valid output signal with a minimum of .2 V difference between the two differential lines.

RULE 4.3.2.1-4:
A differential receiver **MUST** be terminated with 100 Ω in parallel across the differential lines.

RULE 4.3.2.1-5:
The input bias current of a differential receiver **MUST NOT** exceed 1.5 mA at 3 V input.

OBSERVATION 4.3.2.1-6:
Transceivers compliant with EIA-422-A are suitable for use in this application.

4.3.2.2 Single Ended Transceivers

RULE 4.3.2.2-1:
A single ended transmitter **MUST NOT** exceed a maximum low level of .5 V and **MUST** exceed a minimum high level of 2.5 V.

RULE 4.3.2.2-2:
A single ended receiver **MUST** accept any input greater than 1.7 V as a high signal and **MUST** accept any input less than 1.3 V as a low signal.

OBSERVATION 4.3.2.2-3:
Transceivers compliant with EIA-422-A are suitable for use in this application provided the receivers are referenced to a suitable voltage.

4.3.3 Connectors
The MSIB external signals are carried on 37 pin D-type connectors as described in appendix A.

RULE 4.3.3-1:
One end of the cable **MUST** interface with the MSIB out connector and the other must interface with the MSIB in connector as specified in rule 6.2.2.2-1 of chapter 6, *Mechanical Interface*.

4.3.4 Cables

RULE 4.3.4-1:
The voltage rating of the cable **MUST** exceed 30 V rms.

RULE 4.3.4-2:
The maximum single conductor resistance of a cable **MUST NOT** exceed 165 Ω.

RULE 4.3.4-3:
All differential signals **MUST** be connected by a twisted pair of wires with a characteristic impedance of 90 ± 10 Ω.

RULE 4.3.4-4:
The CABLE pin in the connector at each end of a cable **MUST** be connected to a ground pin in the same connector.

RECOMMENDATION 4.3.4-5:
Single conductors should be 26 gauge multistrand (19 × gauge) AWG tinned copper strands.

RECOMMENDATION 4.3.4-6:
An MSIB external cable should be shielded with an inner foil shield for 100% coverage with a drain wire of bare 22 gauge multistrand (7 × 30 gauge) tinned copper, enclosed by an outer braid shield of 36 AWG tinned copper for 85% coverage.

OBSERVATION 4.3.4-7:
The maximum cable length of the recommended cable conductors is limited to about 1 kilometer due to the maximum conductor resistance.

4.3.5 MSIB External Bus Reset

A mainframe's reset algorithm can be implemented to respond solely to only mainframe originated reset or may also include module initiated reset.

RULE 4.3.5-1:
A mainframe **MUST** implement either the mainframe only reset algorithm or the mainframe and module originated reset algorithm.

RECOMMENDATION 4.3.5-2:
The mainframe and module originated reset should be implemented to provide the maximum system capabilities.

4.3.5.1 Mainframe Only Reset Algorithm

The reset algorithm followed by the mainframes for mainframe only reset is described in figure 4-9. The algorithm description is in the form of a state machine as defined in section 1.4.3. This description is not intended as an implementation of the algorithm. An actual implementation would quite likely differ from the state machine shown here. For example, a single state in this description may be implemented as multiple states.

Whenever power is turned off or the mainframe is not ready for operation the state machine is initialized into state A. This results in the assertion of bRst, oRst, and mRst. bRst resets the arbiter and MSIB mainframe translator to their initial states. It also results in the output signals SRDY and DRDY being driven low. This keeps adjacent mainframes from attempting to communicate with this mainframe. oRst causes the RESET output signal to be driven low. This will result in other mainframes in the loop being held in reset. Finally, mRst sends the MSIB internal bus RESET signal to the modules.

Once the mainframe is ready to operate the state machine transitions to state B. In doing so it releases bRst and oRst, resulting in the output signals SRDY, DRDY, and RESET going high. This then allows other mainframes in the system to start running. Note that at this point the output RESET signal is released in spite of what the input RESET signal is doing. If at this point the assertion of the input RESET signal resulted in the assertion of the output RESET signal the system would never come out of reset.

Once in state B the state machine starts looking at the input signals SRDY, DRDY, and RESET. As long as either SRDY or DRDY are false (low) or RESET is true (low), the state machine stays in state B. In this state the modules are held in reset.

Once SRDY and DRDY are true and RESET is false the state machine transitions to state C. No action is taken at this point because the transition might have resulted from a small glitch that occurred at the right time to be sensed by the state machine. To check for this the lines are tested again at least Tdg (150 ns) later. If any of the lines were not stable the machine returns to state B. If the lines remained stable the state machine continues to state E. At this point mRst is negated.

State E is considered the "run" state. In this state the MSIB internal RESET line is false (high) and the mainframe is asserting the MSIB external output signals SRDY and DRDY true and RESET false.

If the previous mainframe in the loop asserts the MSIB external RESET signal then the state machine will transition to state F.

If external RESET remains asserted for at least Tdg (150 ns) after the transition to state F then a transition to state L will occur. At the same time the MSIB mainframe translator and the arbiter will be put into reset.

Tm (150 ns) after entering the L state the state machine will transition to the M state and assert MSIB internal reset. This is the point at which the modules are put into reset.

After Tr (150 ns) the state machine will transition to state N and assert the MSIB external RESET output signal. Note that the assertion of the RESET output signal is delayed from the RESET input signal. This is important to insure that RESET output is asserted for less time than RESET input. This will guarantee that a short assertion pulse in the MSIB external RESET loop will not survive indefinitely. As the pulse travels around the loop it will continue to get shorter until it is finally thrown away as a glitch.

Tnb (150 ns) after entering the N state a transition to the P state will occur and the MSIB mainframe translator and the arbiter will be released from reset. Note that it is important that all the modules have honored the MSIB internal RESET signal by this point. If a module had not honored MSIB internal RESET by this time it could request to transmit a packet and since the arbiter has now been released from reset it would grant that request. The module would then at some later time honer the RESET signal, possibly in the middle of a packet which would generate a packet containing bad data

and/or addresses.

The state machine will remain in state P as long as the MSIB external RESET input signal is asserted. Note that at this point the assertion of the RESET input signal is passed on to the RESET output signal. Since this mainframe is not the mainframe that initiated the system reset it does not break the loop.

Once the RESET input is released the state machine releases the RESET output, releases the modules from reset, and transitions to the run state.

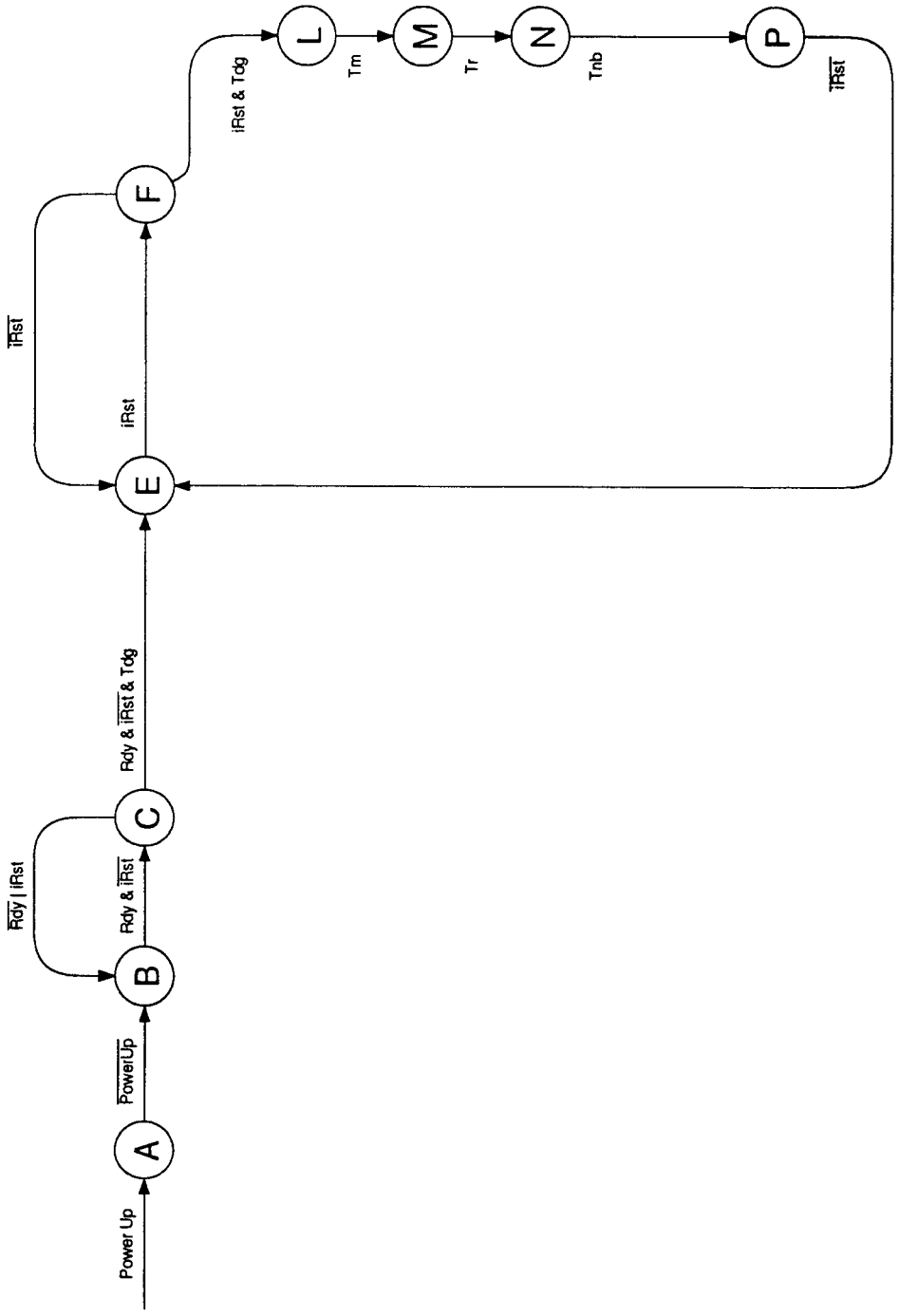


Figure 4-9. Mainframe Only Reset Algorithm

TABLE 4-13. Mainframe Only Reset Algorithm Notation

States:

A	Power up reset is asserted
B	Reset released, wait for external Rdy and iRst signal
C	External signals indicate ready, deglitch them
E	Normal running state, resets released, wait for reset from module or external
F	Either module or external reset asserted, resolve by waiting Tdg and then deciding
L	Reset was from external, reset backplane and wait Tm
M	Assert internal reset and wait Tr
N	Assert reset out and wait Tnb
P	Release backplane reset and wait for external reset in to be released

Conditions:

Power Up	Mainframe not ready to run
Rdy	SRDY and DRDY inputs true (high)
iRst	MSIB external RESET input true (low)

Delays:

Tdg	150 ns - de-glitch time
Tm	150 ns - MSIB external RESET input to MSIB internal RESET
Tr	150 ns - Delay to MSIB external RESET output
Tnb	150 ns - Delay to release of arbiter, MSIB external interface, SRDY & DRDY out

Outputs:

State	Reset Interface	Reset Out	Reset Internal
A	assert	assert	assert
B	-	-	assert
C	-	-	assert
E	-	-	-
F	-	-	-
L	assert	-	-
M	assert	-	assert
N	assert	assert	assert
P	-	assert	assert

Reset Interface	-	assert MSIB external loop SRDY and DRDY outputs
	assert	reset external interface and arbiter and do not assert MSIB external loop SRDY and DRDY outputs
Reset Out	-	do not assert MSIB external loop reset output
	assert	assert MSIB external loop reset output
Reset Internal	-	do not assert MSIB internal bus reset
	assert	assert MSIB internal bus reset

4.3.5.2 Mainframe and Module Originated Reset Algorithm

The reset algorithm followed by the mainframes is described in figure 4-10. The algorithm description is in the form of a state machine as defined in section 1.4.3. This description is not intended as an implementation of the algorithm. An actual implementation would quite likely differ from the state machine shown here. For example, a single state in this description may be implemented as multiple states.

Whenever power is turned off or the mainframe is not ready for operation the state machine is driven into state A. This results in the assertion of bRst, oRst, and mRst. bRst resets the arbiter and MSIB Mainframe Translator to their initial states. It also results in the output signals SRDY and DRDY being driven low. This keeps adjacent mainframes from attempting to communicate with this

mainframe. oRst causes the RESET output signal to be driven low. This will result in other mainframes in the loop being held in reset. Finally, mRst sends the MSIB internal bus RESET signal to the modules.

Once the mainframe is ready to operate the state machine transitions to state B. In doing so it releases bRst and oRst, resulting in the output signals SRDY, DRDY, and RESET going high. This then allows other mainframes in the system to start running. Note that at this point the output RESET signal is released in spite of what the input RESET signal is doing. If at this point the assertion of the input RESET signal resulted in the assertion of the output RESET signal the system would never come out of reset.

Once in state B the state machine starts looking at the input signals SRDY, DRDY, and RESET. As long as either SRDY or DRDY are false (low) or RESET is true (low), the state machine stays in state B. In this state the modules are held in reset.

Once SRDY and DRDY are true and RESET is false the state machine transitions to state C. No action is taken at this point because the transition might have resulted from a small glitch that occurred at the right time to be sensed by the state machine. To check for this the lines are tested again at least Tdg (150 ns) later. If any of the lines were not stable the machine returns to state B. If the lines remained stable the state machine continues to state D. At this point MF is negated. This will result in the MSIB internal RESET signal going high (false) if no module is holding it low. If any module is holding it low the other modules will remain in reset and the state machine will stay in state D.

Once all modules have released the MSIB internal RESET line the state machine will proceed to state E. This is considered the "run" state. In this state the MSIB internal RESET line is false (high) and the mainframe is asserting the MSIB external output signals SRDY and DRDY true and RESET false.

If any module asserts the MSIB internal RESET line or if the previous mainframe in the loop asserts the MSIB external RESET signal then the state machine will transition to state F.

If the signal that caused the transition to state F is still present after the de-glitch time Tdg then a transition to either state G or state L will occur.

If a module is asserting MSIB internal RESET then the transition will be to state G. At this time the MSIB mainframe translator and the arbiter will be put into reset. This will also result in the mainframe asserting its SRDY and DRDY output lines.

After Tr (150 ns) a transition to state H will occur. At this time the mainframe will assert its MSIB external RESET output line.

After Tnb (150 ns) a transition to state J will occur and the MSIB mainframe translator and the arbiter will be released from reset.

As long as any module continues to assert the MSIB internal RESET signal the state machine will remain in state J. Once all modules have released RESET the state machine will transition to state K and the MSIB external RESET output line will be released.

The state machine will remain in state K until the MSIB external RESET input line is released. Note that at this point the fact that the MSIB external RESET input is asserted does not result in the RESET output being asserted. In other words, the reset loop is broken at this point. The fundamental concept is this: The mainframe that initiated the reset process must break the reset loop by ignoring its RESET input in order that it be able to release the system from reset.

Once the RESET input is released the state machine returns to state E, the run state.

Now let's assume a transition from state E to state F occurred because the MSIB external RESET input was asserted. If the signal remains asserted for Tdg (150 ns) after the transition to state F then a transition to state L will occur. At the same time the MSIB mainframe translator and the arbiter will be put into reset.

Tm (150 ns) after entering the L state the state machine will transition to the M state and assert MSIB internal reset. This is the point at which the modules are put into reset.

After Tr (150 ns) the state machine will transition to state N and assert the MSIB external RESET output signal. Note that the assertion of the RESET output signal is delayed from the RESET input signal. This is important to insure that RESET output is asserted for less time than RESET input. This will guarantee that a short assertion pulse in the MSIB external RESET loop will not survive indefinitely. As the pulse travels around the loop it will continue to get shorter until it is finally thrown away as a glitch.

Tnb (150 ns) after entering the N state a transition to the P state will occur and the MSIB mainframe translator and the arbiter will be released from reset. Note that it is important that all the modules have honored the MSIB internal RESET signal by this point. If a module had not honored MSIB internal RESET by this time it could request to transmit a packet and since the arbiter has now been released from reset it would grant that request. The module would then at some later time honer the RESET signal, possibly in the middle of a packet which would generate a packet containing bad data and/or addresses.

The state machine will remain in state P as long as the MSIB external RESET input signal is asserted. Note that at this point the assertion of the RESET input signal is passed on to the RESET output signal. Since this mainframe is not the mainframe that initiated the system reset it does not break the loop.

Once the RESET input is released the state machine releases the RESET output, releases the modules from reset, and transitions to the run state.

RULE 4.3.5.2-1:

The MSIB external reset generator **MUST** follow the sequence of events shown in figure 4-10.

RULE 4.3.5.2-2:

The MSIB external reset generator **MUST** include delays of no less than the the delays shown in figure 4-10.

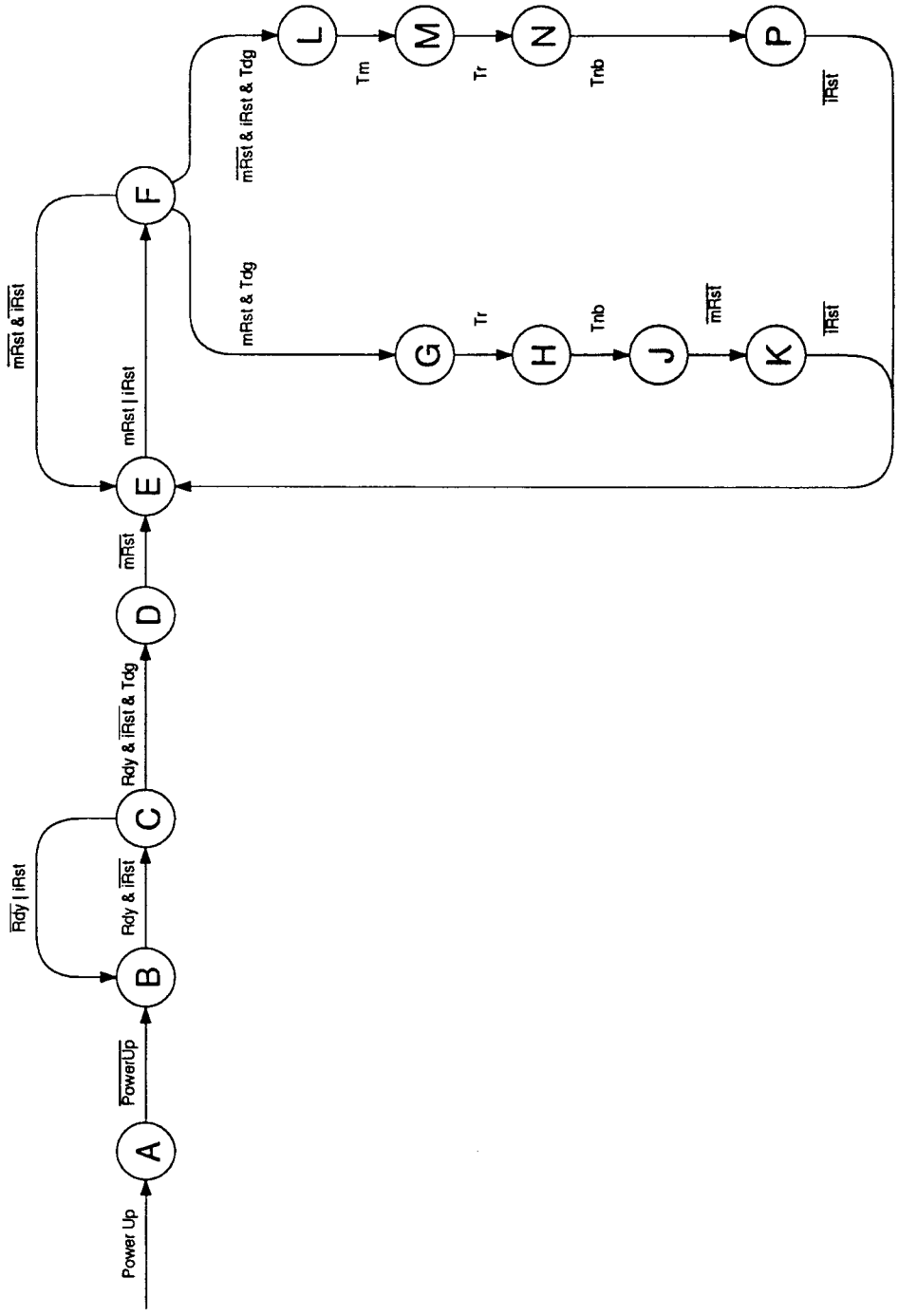


Figure 4-10. Mainframe and Module Originated Reset Algorithm

TABLE 4-14. Mainframe and Module Originated Reset Algorithm Notation

States:

A	Power up reset is asserted
B	Reset released, wait for external Rdy and iRst signal
C	External signals indicate ready, deglitch them
D	External signals remained ready for TDG, wait for module asserted reset to released
E	Normal running state, resets released, wait for reset from external
F	External reset asserted, deglitch
G	Reset was from module, assert backplane reset and wait TR
H	Assert reset out and wait Tnb
J	Release backplane reset and wait for module to release internal reset
K	Internal reset released, release reset out and wait for release of reset in
L	Reset was from external, reset backplane and wait Tm
M	Assert internal reset and wait Tr
N	Assert reset out and wait Tnb
P	Release backplane reset and wait for external reset in to be released

Conditions:

Power Up	Mainframe not ready to run
Rdy	SRDY and DRDY inputs true (high)
iRst	MSIB external RESET input true (low)

Delays:

Tdg	150 ns - de-glitch time
Tm	150 ns - MSIB external RESET input to MSIB internal RESET
Tr	150 ns - Delay to MSIB external RESET output
Tnb	150 ns - Delay to release of arbiter, MSIB external interface, SRDY & DRDY out

Outputs:

State	Reset Interface	Reset Out	Reset Internal
A	assert	assert	assert
B	-	-	assert
C	-	-	assert
D	-	-	-
E	-	-	-
F	-	-	-
G	assert	-	-
H	assert	assert	-
J	-	assert	-
K	-	-	-
L	assert	-	-
M	assert	-	assert
N	assert	assert	assert
P	-	assert	assert

Reset Interface	-	assert MSIB external loop SRDY and DRDY outputs
	assert	reset external interface and arbiter and do not assert MSIB external loop SRDY and DRDY outputs
Reset Out	-	do not assert MSIB external loop reset output
	assert	assert MSIB external loop reset output
Reset Internal	-	do not assert MSIB internal bus reset
	assert	assert MSIB internal bus reset

5. COMMUNICATION PROTOCOL

The MMS communication protocol defines how communication occurs over MSIB. It defines how packet information provided by a module's MSIB hardware interface should be processed by a module's protocol interface. Figure 5-1 shows the relationships between a module's MSIB hardware interface, protocol interface, and module processes. Several links can be processed through a module's MSIB interface at the same time. Communication control provided by the MSIB protocol interface provides the mechanism for a logical module to manage these links. Data specific to a particular link can be passed through to the appropriate module process by the MSIB protocol interface. Common system functions such as module identification are defined by MSIB commands. Module processes can obtain information about other modules using these MMS defined functions.

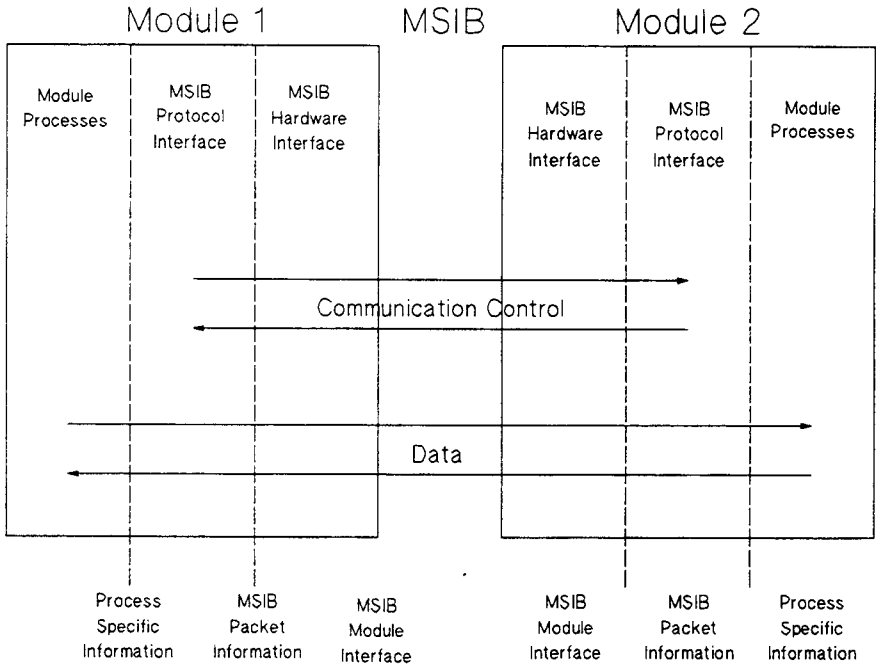


Figure 5-1. MSIB Protocol Relationship to Module Functions

5.1 Protocol Revision

The communication protocol revision is maintained independent of the MMS Specification revision. The current MMS communication *Protocol Revision is 2.2.*

5.2 Overview

This section provides an overview of the MSIB Communication Protocol as an introduction. Some details have been omitted in order to simplify the presentation. Refer to the descriptions in the following sections for details needed for implementation.

5.2.1 Use of MSIB

MSIB is used for communications between modules in a Modular Measurement System. Several kinds of messages can be sent between logical modules using MSIB. Some examples of messages sent over MSIB are: control of another module or transferring measurement data from one module to the other. Figure 5-1 shows the relationship of these messages, indicated as data, to the MSIB Protocol, indicated as communication control.

MSIB Protocol controls the flow of data between processes in two logical modules. This protocol is designed so that the mechanics of communication can be transparent to higher level processes running in logical modules.

5.2.2 MSIB Commands Overview

MSIB Commands are used to communicate messages outside of the context of a data message. MSIB commands are used to control links, perform common functions, and perform module dependent functions. The MSIB hardware indicates if a packet is an MSIB command so that MSIB commands can be easily differentiated from data messages.

5.2.3 Tagged Links Overview

Communication between logical modules occurs primarily using tagged links. One or more tagged links may be used for communication between two logical modules. A logical module may use several tagged links at the same time for communicating to several other modules. Tagged links are established as a specific type, such as graphics or control. A logical module identifies a tag for each link to associate the data stream with the link. This allows low level drivers to determine which process to direct data.

There are always two modules that participate in a link, the initiator and the responder. As the first step in setting up a tagged link the initiator sends an **ESTABLISH TAGGED LINK** MSIB command to the responder. The module receiving one of these commands may either accept or reject the link. If the module is willing to accept the link it responds with the **ACCEPT LINK** MSIB command. If it is not it responds with the **REJECT LINK** MSIB command. If the link is accepted, the link initiator next sends the tag used to identify data sent to it, using the **IDENTIFY LINK INITIATOR** MSIB command. The link responder also sends a tag used to identify data sent to it, using the **IDENTIFY LINK RESPONDER** MSIB command. Now the link may be used for communication between the two modules. The **SELECT LINK** MSIB command is first sent to identify which link to direct the data message. When data is for another link a **SELECT LINK** MSIB command is sent to change the destination link. The initiator and the responder can independently select a destination link.

Either module may choose to break the link. This is done by sending the **BREAK LINK** MSIB command. A module with an active link that receives the **BREAK LINK** MSIB command has no choice but accept the break by responding with the **ACCEPT BREAK LINK** MSIB command.

The initiator of a link may lock a link by sending the responder a **LOCK LINK** MSIB command. A link that is locked may only be broken by the initiator, The initiator unlocks the link with the **UNLOCK**

LINK MSIB command.

5.3 Packets

The MSIB module interface provides information to the protocol interface one packet at a time. Table 5-1 summarizes the packet information that is available to the module's MSIB protocol interface. The packet information will arrive to the protocol interface as a serial stream in proper order and free of transmission errors.

TABLE 5-1. MSIB Packet Information

Packet Item	Size	Comments
TO ADDRESS	8 bits	address of packet destination
FROM ADDRESS	8 bits	address of packet origin
BYTE/$\overline{\text{WORD}}$	1 bit	indicates 8 or 16 bit data size
COMMAND	1 bit	indicates to interpret as a command
DATA	8/16 bits	data size indicated by BYTE/$\overline{\text{WORD}}$

The COMMAND bit determines whether the packet is an MSIB command or a data message. MSIB commands are used for the following purposes:

- control of the communication process,
- for module-independent common MMS functions, or
- for module dependent purposes.

The MSIB communication protocol is implemented using MSIB commands.

RULE 5.3-1:

The transmitting module **MUST** use the BYTE/$\overline{\text{WORD}}$ bit to indicate whether 8-bits or 16-bits of data is contained in a packet.

RULE 5.3-2:

The receiving module **MUST** interpret the received data as 8-bits or 16-bits based on the state of the BYTE/$\overline{\text{WORD}}$ bit.

RULE 5.3-3:

A packet containing two bytes of data **MUST** be sent with the first byte in DATA 1, the second byte in DATA 2, and the B/W bit false.

RULE 5.3-4:

A packet containing one byte of data **MUST** be sent with the data byte in DATA 1 and the B/W bit true.

PERMISSION 5.3-5:
A packet containing one byte of data **MAY** be sent with any value in DATA 1.

PERMISSION 5.3-6:
Data being sent is treated as a continuous stream of bytes and **MAY** be sent using any combination of byte and word packets.

RECOMMENDATION 5.3-7:
Data should be sent two bytes to a packet whenever possible.

RULE 5.3-8:
The DATA 1 field in a packet received with the B/W bit true **MUST NOT** be treated as part of the data stream.

RULE 5.3-9:
A packet received with the B/W bit false **MUST** be interpreted as having two data bytes with the first byte in DATA 1 and the second byte in DATA 2.

RULE 5.3-10:
Received data **MUST** be treated as a continuous stream of data regardless of the combination of byte and word packets in which it is contained.

5.3.1 Data Packets

OBSERVATION 5.3.1-1:
Packets sent with command bit false are data messages defined by the context of the communication.

5.3.2 Command Packets

RULE 5.3.2-1:
Packets sent with COMMAND true with data in the range 0000H through BFFFH are MSIB commands which **MUST** be interpreted as an MSIB command reserved by this specification.

RULE 5.3.2-2:
The data contained in a packet received with the CMD bit true **MUST** be interpreted as an MSIB command.

OBSERVATION 5.3.2-3:
Packets sent with COMMAND bit true with data in the range C000H through FFFFH are MSIB commands available for specific applications.

RECOMMENDATION 5.3.2-4:
Whenever possible, data messages should be used in preference to packets sent with COMMAND true with data in the range C000H through FFFFH.

RULE 5.3.2-5:
For commands that are not recognized, an **UNRECOGNIZED COMMAND** MSIB command **MUST** be sent by the receiving module to the module that sent the command. The receiving module **MUST NOT** report any other error condition.

RECOMMENDATION 5.3.2-6:
The **UNRECOGNIZED COMMAND** MSIB command should not be used to determine if a capability is implemented in another module.

RECOMMENDATION 5.3.2-7:
The protocol revision of a module should be determined using a **SEND MODULE ID** MSIB command. If the protocol revision is greater than 2.0 the **SEND CAPABILITY** MSIB command should be used to determine the exact capabilities of a module.

5.3.3 Command Responses

Some MSIB commands are queries which require a response. A logical module uses the **COMMAND RESPONSE** MSIB command to communicate this response. The only exception is the **SEND STATUS** and **STATUS** MSIB commands that work together reporting the status byte.

RULE 5.3.3-1:
MSIB command responses **MUST** be communicated one byte at a time using the **COMMAND RESPONSE** MSIB command.

RULE 5.3.3-2:
The last byte of a **COMMAND RESPONSE** MSIB command **MUST** be terminated by the **END COMMAND RESPONSE** MSIB command.

RECOMMENDATION 5.3.3-3:
Since it is not possible to distinguish between different MSIB command responses from the same address, an MSIB command query should not be sent if a previous query has been sent and the **END COMMAND RESPONSE** MSIB command for that query has not been received.

5.4 Illegal Communications

RULE 5.4-1:
Packets received that do not meet the requirements for legal MSIB communication **MUST** generate an illegal communication error.

RULE 5.4-2:
An MSIB command which is not recognized by the module **MUST NOT** be treated as an illegal communication.

RECOMMENDATION 5.4-3:
When an illegal communication is detected, the logical module should report the condition through its own error reporting mechanism.

RULE 5.4-4:
When an illegal communication is detected, the logical module **MUST** send the **ILLEGAL COMMUNICATION** MSIB command to the originator of the illegal communication.

RULE 5.4-5:
When an illegal communication is detected by a logical module, it **MUST** go to the idle state in all links with the originating module.

RULE 5.4-6:
When a logical module receives an **ILLEGAL COMMUNICATION** MSIB command, it **MUST** go to the idle state in all links with the sending module unless rule 5.4-7 applies.

RULE 5.4-7:
A logical module with links in the Initiator Opening (IO) or Initiator Pending (IP) states **MUST NOT** affect the state of those links in response to an **ILLEGAL COMMUNICATION** MSIB command. Refer to section 5.6.2, *Link States*, for further information.

OBSERVATION 5.4-8:
When an illegal communication occurs between two modules, there may be a loss in the synchronization of the two modules. Both modules go to an idle state without using the normal methods of closing the conversations between them.

RULE 5.4-9:
When there is no link established or selected, a data packet **MUST** be processed as an illegal communication.

RULE 5.4-10:
An **ILLEGAL COMMUNICATION** MSIB command **MUST** only be generated as defined by this specification.

5.5 Link Data Streams

Links are used for communication between modules in MMS. A link consists of two data streams, one in each direction between two modules. Multiple communications can take place independently between modules over the MSIB interface using one link per communication. Figure 5-2 is an example of two modules using links for communication between processes.

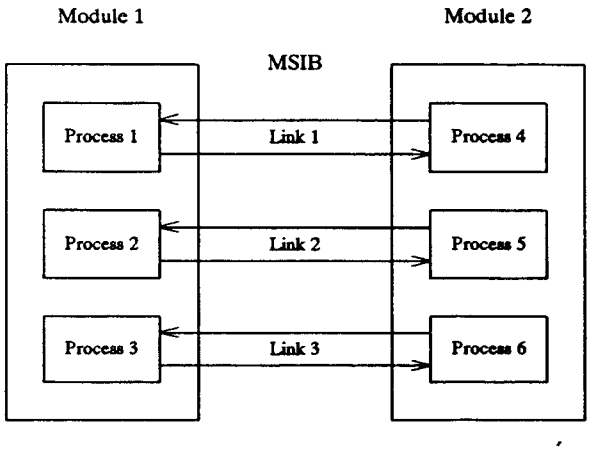


Figure 5-2. MSIB Link Communication

Packets may be output for any of the links, multiplexed as determined by the sending module. Packets are associated with the appropriate link as determined by MSIB commands. The sending module selects the link data stream the following packets belong to. The receiving module can then route packets to the appropriate process based on the association with a particular link data stream.

5.5.1 Selecting a Data Stream

The sending module sends MSIB commands to tell the receiving module which link the following data belongs to. There are two methods that can be used to identify link data streams, tag or non-tagged.

OBSERVATION 5.5.1-1:

The primary criteria for choosing between different data streams is the **FROM ADDRESS** accompanying every packet. When there is more than one link between two modules, additional information is needed to select between the data streams.

RULE 5.5.1-2:

When a data stream from a particular module has been selected, the receiving module **MUST** remember the selection until the next selection takes place.

OBSERVATION 5.5.1-3:

The selection of a data stream only refers to communication in one direction in a link. The other module could have selected a data stream from another link for the data it is sending.

5.5.1.1 Tagged Links

Tags are exchanged between two modules for future identification of links. At a later time, the tag is used to select a particular link. The selected link will receive data or be affected by a subsequent MSIB command that refers to the link.

RULE 5.5.1.1-1:
The data stream set up by a tagged link **MUST** be selected using the **SELECT LINK** MSIB command.

OBSERVATION 5.5.1.1-2:
Establishing a tagged link has no effect on the selected data stream.

RULE 5.5.1.1-3:
A unique tag **MUST** be used to identify each link with a specific logical module.

RULE 5.5.1.1-4:
Data messages and the following link specific MSIB commands **MUST** only be applied to the selected tagged link: **END, SEND STATUS, STATUS, ACCEPT BREAK LINK, BREAK LINK, LINK LOCAL, LINK REMOTE, LOCK LINK, UNLOCK LINK, TRANSMIT ON,** and **TRANSMIT OFF.**

5.5.1.2 Non-Tagged Links
Non-tagged links provide a simple mechanism for communication with only a single pair of data streams between a pair of modules. Keyboard, graphics, or control links may be established using the **ESTABLISH NON-TAGGED LINK** MSIB command.

RULE 5.5.1.2-1:
A logical module **MUST** support non-tagged links if it has an MSIB interface.

OBSERVATION 5.5.1.2-2:
There is no way to separate the data streams of different non-tagged links. If multiple non-tagged links are used, separation of the data streams is handled at a higher level in the module's software than would be necessary with tagged links.

OBSERVATION 5.5.1.2-3:
Non-tagged links were implemented on early modules that did not have tagged link capability. Non-tagged links are important to maintain compatibility with the installed base of MMS modules.

5.6 Link Operation

Links provide for orderly operation of conversations between Modular Measurement System modules. The module initiating the link is referred to as the link initiator. The module accepting a link is referred to as the link responder.

Management of links is done using MSIB commands. The use of these commands is the same regardless of the type of link being used.

There are several types of links. The link types specify the language to be used in the data stream communications and the method of identifying that data stream.

Links may be set up in either tagged or non-tagged form. Tagged links provide a specific tag that is used to separate data streams when there are multiple links between a pair of modules. Non-tagged links are the original link form used in MMS modules.

RULE 5.6-1:
A link **MUST** be set up between modules before communication using data messages and link specific commands takes place.

RULE 5.6-2:
For modules at a protocol revision greater than or equal to 2.0, tagged links **MUST** be implemented for all link types that the module supports.

OBSERVATION 5.6-3:
Modules prior to protocol revision 2.0 do not implement tagged links.

RULE 5.6-4:
If two modules both have tagged link capability, then tagged links **MUST** be used for all links between the two modules.

RULE 5.6-5:
Non-tagged links **MUST** only be used for keyboard, graphics, or control.

5.6.1 Link Types

RULE 5.6.1-1:
Link types 0H through BH are reserved by this specification.

OBSERVATION 5.6.1-2:
Link types CH through FH are available for module specific uses.

5.6.1.1 Control Link
A control link is used by one module to control the functions of another module. The initiator of a control link always sends commands to the responder in the responder's control language.

OBSERVATION 5.6.1.1-1:
The language used over control links will vary with different modules. This requires the initiating module to know the identity of a particular module before communicating with it. This can be determined using the **SEND MODULE ID** MSIB command.

5.6.1.2 Data Link
A data link is used to communicate module dependent data not associated with the direct control of the module. The meaning of the data is implied by specific module design. An example might be measurement data that is being acquired and then sent to another module for additional processing.

OBSERVATION 5.6.1.2-1:
There is no implication as to which direction data should flow as there is with other link types. It is possible for a data link to define a data stream in one direction only.

OBSERVATION 5.6.1.2-2:
A data link is only allowed for tagged links. See **ESTABLISH NON-TAGGED LINK** and **ESTABLISH TAGGED LINK** descriptions in section 5.18.

5.6.1.3 Registered Links
A registered link is a link which has been associated with a particular language for a common MMS system function. This allows access of common MMS system functions at known link numbers. A registered link number is assigned by the MMS Consortium for languages that are useful for general application in the MMS system.

5.6.1.3.1 Keyboard Link
A keyboard link is a registered link used to provide manual user input in an MMS system.

5.6.1.3.2 Graphics Link
A graphics link is a registered link used to communicate the status of a module to the user in an MMS system.

5.6.1.3.3 Storage Link
A storage link is a registered link used by a module to gain access to common storage in an MMS system.

5.6.2 Link States

All link types are governed by the same pair of state diagrams, figure 5-3 for the initiator and figure 5-4 for the responder. Tables 5-2, 5-3, and 5-4 define the symbols used in these diagrams.

There are eight MSIB commands used for link management:

- **ESTABLISH TAGGED LINK**
- **ESTABLISH NON-TAGGED LINK**
- **ACCEPT LINK**
- **IDENTIFY LINK INITIATOR**
- **IDENTIFY LINK RESPONDER**
- **REJECT LINK**
- **BREAK LINK**
- **ACCEPT BREAK LINK**

Links are available for communication when the initiator is in the Initiator Active (IA) state and the responder is in either the Responder Active (RA) or Responder Locked (RL) state. When the responder is in the Responder Locked state it can not close the link on its own initiation.

RULE 5.6.2-1:

If a module receives any of the MSIB commands used for link management that are not defined for the current state of the appropriate link state diagram the module **MUST** respond with an **ILLEGAL COMMUNICATION** MSIB command.

RULE 5.6.2-2:

A logical module **MUST** respond with the **REJECT LINK** MSIB command to any establish link command (tagged or non-tagged) when the link type is not implemented in the module.

RULE 5.6.2-3:

A logical module **MUST** implement links in accordance with the initiator and responder state diagrams shown in figure 5-3 and figure 5-4.

RULE 5.6.2-4:

If an initiator needs to set up more than one tagged link of the same type with another module, it **MUST** establish the links one at a time. The initiator **MUST NOT** be in the **IO**, **IT**, or **IP** state for the same type link.

PERMISSION 5.6.2-5:

An initiator **MAY** set up multiple tagged links with another module without waiting for each to be accepted, provided the links are of different types.

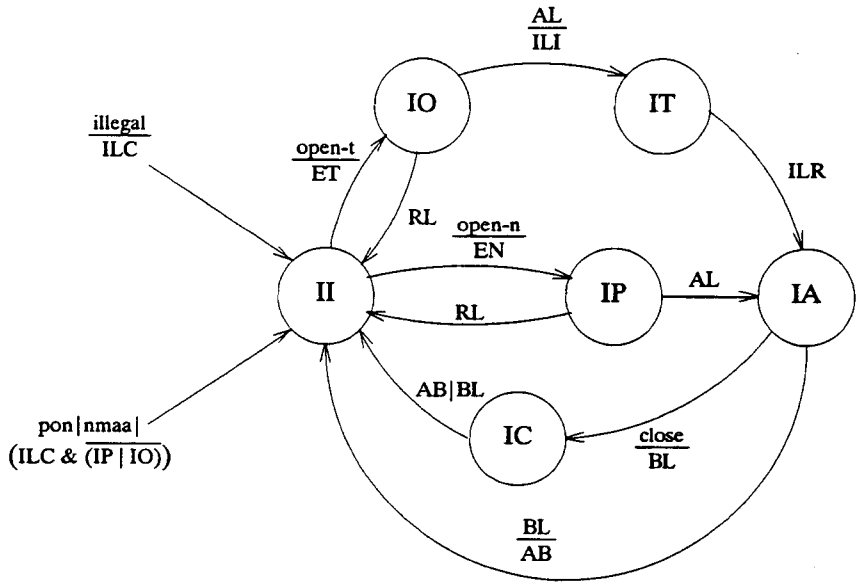


Figure 5-3. Link Initiator State Diagram

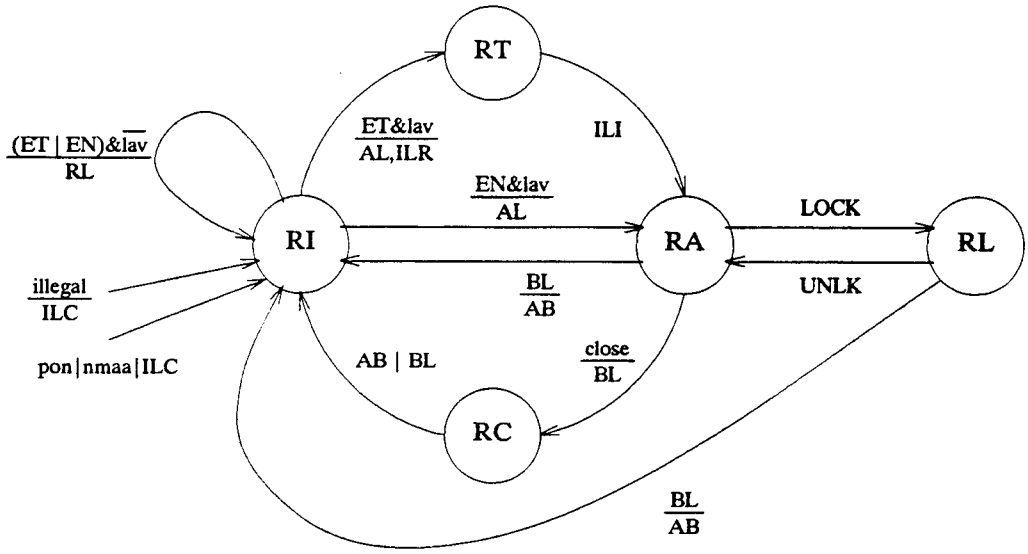


Figure 5-4. Link Responder State Diagram

TABLE 5-2. Link States

Mnemonic	Name	Meaning
II	Initiator idle	There is no link
IO	Initiator opening	The initiator has sent an establish tagged link and is waiting for an accept
IP	Initiator pending	The initiator has sent an establish non-tagged link and is waiting for an accept
IT	Initiator tag	Initiator is waiting for link tag from responder
IA	Initiator active	The link is established
IC	Initiator closing	Initiator has sent a break link and is waiting for an accept
RI	Responder idle	There is no link
RT	Responder tag	Responder is waiting for link tag from initiator
RA	Responder active	The link is established
RL	Responder locked	The link is established and locked
RC	Responder closing	Responder has sent a break link and is waiting for an accept

TABLE 5-3. State Transition Actions

Mnemonic	Meaning
ET	Send MSIB establish tagged link command
EN	Send MSIB establish non-tagged link command
AL	Send MSIB accept link command
RL	Send MSIB reject link command
ILI	Send MSIB identify link initiator command
ILR	Send MSIB identify link responder command
ILC	Send MSIB illegal communication command
BL	Send MSIB break link command
AB	Send MSIB accept break link command

TABLE 5-4. State Transition Conditions

Mnemonic	Meaning
ET	Establish tagged link MSIB command received
EN	Establish non-tagged link MSIB command received
AL	Accept link MSIB command received
RL	Reject link MSIB command received
ILI	Identify link MSIB initiator command received
ILR	Identify link MSIB responder command received
BL	Break link MSIB command received
AB	Accept break link MSIB command received
LOCK	Lock link MSIB command received
UNLC	Unlock link MSIB command received
ILC	Illegal communication MSIB command received
pon	System reset (SYSRST*) is released
illegal	An illegal MSIB communication has been detected
nmaa	No module at address detected by MSIB interface device
lav	Link available: This module is ready to accept this type of link.
open-t	This module wishes to establish a tagged link
open-n	This module wishes to establish a non-tagged link
close	This module wishes to close a link
tag	This link is a tagged link

5.6.2.1 Link Initiator Responsibilities

RULE 5.6.2.1-1:
For each active link, a link initiator **MUST** support the link's functions with an individual initiator state machine.

RULE 5.6.2.1-2:
When the link initiator enters the initiator active state (IA), all data stream buffers **MUST** be empty and all parsing mechanisms **MUST** be in their initial state.

SUGGESTION 5.6.2.1-3:
A link initiator in the initiator active (IA) state should wait until the end of a logical message before sending a **BREAK LINK** MSIB command. This will reduce the possibility of generating errors during the process of closing the link.

RULE 5.6.2.1-4:
A link initiator **MUST NOT** send data messages or link specific commands to the link responder except in the initiator active (IA) state.

RULE 5.6.2.1-5:
A link initiator **MUST** accept data messages and link specific commands from the link responder in the initiator active (IA) and initiator closing (IC) states.

OBSERVATION 5.6.2.1-6:
When the link initiator is in the initiator active (IA) state and a **BREAK LINK** MSIB command is received no further query responses should be expected from the link responder.

5.6.2.2 Link Responder Responsibilities

RULE 5.6.2.2-1:
For each active link, a link responder **MUST** support the link's functions with an independent responder state machine.

OBSERVATION 5.6.2.2-2:
There is no case that a logical module would respond to an **ESTABLISH LINK** or **ESTABLISH NON-TAGGED LINK** with an **ILLEGAL COMMUNICATION**. The only response is **ACCEPT LINK** or **REJECT LINK**.

OBSERVATION 5.6.2.2-3:
A module will have some limit on its ability to accept links depending upon the processing resources available to it. When this limit is exceeded, it still must process the request as an input to another state diagram which has only one state. This one state is the responder idle state.

SUGGESTION 5.6.2.2-4:
For most link types, it is desirable to honor the most recent request for a link. Since a link request is likely to be generated as the result of a user action, the module will have a good chance of satisfying the user's intent if it honors the most recent request. This can be handled by closing another link. The other link is closed by generating the local message "close" to that link state machine. When that link completes closing, the link could be granted to the most recent initiator.

RULE 5.6.2.2-5:
When the link responder enters the responder active state (RA), all data stream buffers **MUST** be empty and all parsing mechanisms **MUST** be in their initial state.

OBSERVATION 5.6.2.2-6:
When in the responder lock (RL) state, the module is not allowed to respond to an internal "close" message.

OBSERVATION 5.6.2.2-7:
When the link initiator is in the initiator active (IA) state, the link responder could send a **BREAK LINK** MSIB command after the link initiator has sent a **LOCK LINK** MSIB command. This could occur before the transition from responder active (RA) to responder locked (RL).

SUGGESTION 5.6.2.2-8:
A link responder in the responder active (RA) state should wait until the end of a logical message before sending a **BREAK LINK** MSIB command. This will reduce the possibility of generating errors during the process of closing the link.

RULE 5.6.2.2-9:
A link responder **MUST NOT** send data messages or link specific commands to the link initiator except in the responder active (RA) and responder locked (RL) states.

RULE 5.6.2.2-10:
A link responder **MUST** accept data messages and link specific commands from the link initiator in the responder active (RA), responder locked (RL), and responder closing (RC) states.

OBSERVATION 5.6.2.2-11:
When the link responder is in the responder active (RA) or responder locked (RL) state and a **BREAK LINK** MSIB command is received no further query responses should be expected from the link initiator.

5.7 Transmit Pacing

Transmit pacing allows a receiving module to limit the data flow from a particular tagged link when it can not keep up with a transmitting module. When a receiving module can not receive as fast as the transmitting module, its input buffer fills up. This will result in the receiving module holding off further packets at its MSIB interface. When it is important to receive packets from multiple links, transmit pacing protocol provides better control of the input data streams. There are three MSIB commands used for transmit pacing:

- TRANSMIT ON

- TRANSMIT OFF
- NULL

When a receiving module needs to stop the data transfer from a particular tagged link it selects that link and sends a **TRANSMIT OFF** MSIB command. This is followed by two **NULL** MSIB commands. The acceptance of the second **NULL** MSIB command indicates the transmitting module has acknowledged the **TRANSMIT OFF** MSIB command and no further data will be sent on that link. When a **TRANSMIT ON** MSIB command is sent transmission will continue.

RECOMMENDATION 5.7-1:
Transmit pacing should be implemented in a logical module since it benefits both the module and other modules communicating with it.

RULE 5.7-2:
Transmit pacing commands **MUST** only be used with tagged links.

RECOMMENDATION 5.7-3:
A receiving module should check to see if the transmitting module has transmit pacing, using the **SEND CAPABILITY** MSIB command, before sending any transmit pacing MSIB commands.

RULE 5.7-4:
When a tagged link is established both modules **MUST** enable their outputs as if the **TRANSMIT ON** MSIB command had been sent.

RECOMMENDATION 5.7-5:
If the receiving module is capable of using transmit pacing and the transmitting module has transmit pacing capability, the receiving module should use transmit pacing. A multiple module system may require transmit pacing to guarantee proper operation.

OBSERVATION 5.7-6:
A receiving module may send the **TRANSMIT ON** and **TRANSMIT OFF** MSIB commands to control the transmitting module with transmit pacing capability, even though the receiving module is not capable of accepting these commands.

OBSERVATION 5.7-7:
Both the initiator and the responder of a tagged link may use the **TRANSMIT ON** and **TRANSMIT OFF** MSIB commands.

RULE 5.7-8:
The transmitting module **MUST NOT** accept more than one packet from the receiving module after receiving a **TRANSMIT OFF** MSIB command, until it has disabled output to that link.

RULE 5.7-9:
After the transmitter receives a **TRANSMIT OFF** it **MUST** stop sending output, without requiring the receiver to accept any additional packets.

OBSERVATION 5.7-10:
Acceptance of the second **NULL** packet by the transmitting module indicates that output has been disabled to that link.

RULE 5.7-11:
When the transmitting module receives a **TRANSMIT ON** MSIB command it **MUST** enable its outputs for that link.

RULE 5.7-12:
The receiving module **MUST** consider the output enabled until the **TRANSMIT OFF** and two **NULL** MSIB commands have been sent.

OBSERVATION 5.7-13:
A particular implementation of an MSIB hardware interface might require a receiving module to stop accepting input from any address until the transmit off is acknowledged.

RULE 5.7-14:
After the transmitting module disables its output to a link, it **MUST** resume accepting packets from that link.

OBSERVATION 5.7-15:
The second **NULL** MSIB command successfully sent after a **TRANSMIT OFF** MSIB command indicates a transmit off acknowledgement. After this acknowledgement is received a module will not receive more than one additional packet from the sending module. This last packet might be a packet being transmitted during the transmit off. There may be an additional packet already accepted by the receiving module in its input buffer as well.

RECOMMENDATION 5.7-16:
The time between receiving a **TRANSMIT OFF** MSIB command and disabling output should be kept as short as possible. A long response time will degrade system performance.

RULE 5.7-17:
The **TRANSMIT ON** and **TRANSMIT OFF** MSIB Commands **MUST** be accepted regardless off the effect of any previous **TRANSMIT ON** or **TRANSMIT OFF** sent or received on a link.

OBSERVATION 5.7-18:
The **TRANSMIT ON** and **TRANSMIT OFF** MSIB Commands are immune to the effects of previous **TRANSMIT ON** or **TRANSMIT OFF** MSIB Commands. This assures that the packet flow to a link can be controlled in any situation.

RULE 5.7-19:
More than one **TRANSMIT ON** MSIB command **MUST** be treated the same way as one **TRANSMIT ON** MSIB Command until a **TRANSMIT OFF** has been received.

RULE 5.7-20:
More than one **TRANSMIT OFF** MSIB command **MUST** be treated the same way as one **TRANSMIT OFF** MSIB command until a **TRANSMIT ON** has been received.

5.8 Remote Control

There are several possible sources that can control a logical module's operation. Remote control communications are possible using an MSIB control link, IEEE 488.1, or some other control source. Manual operation is accomplished over the keyboard and graphics links. These various sources of control need to be taken into account in the design of a module. A module, because of its own internal processing limitations, will have a limit to the number of remote communications it can handle simultaneously.

RECOMMENDATION 5.8-1:
A logical module should respond in the same language over its IEEE 488.1 interface that it responds to over its control link.

RULE 5.8-2:
A logical module **MUST** disable manual operation if any control source is inhibiting manual operation. Examples are MSIB control link remote or IEEE 488.1 in remote.

RECOMMENDATION 5.8-3:
When manual control is disabled, the menu keys should be blanked if they are currently displayed.

RULE 5.8-4:
When no control source is inhibiting manual operation, the instrument **MUST** enable manual operation and redisplay the menu keys if previously blanked.

RULE 5.8-5:
The **RETURN TO LOCAL** MSIB command **MUST** generate a return to local message to the IEEE 488.1 remote local state function. This command **MUST NOT** affect the state of MSIB link remote states.

5.9 MSIB Remote/ Local Control

An automatic test program controlling instruments often will want to prevent operators from using manual controls to interfere with the test. IEEE 488.1 provides this mechanism with the remote local lockout state of the remote local function. A similar capability exists with a control link over the MSIB.

RULE 5.9-1:
If a module implements the MSIB link remote capability, the control link **MUST** be in the local state when the link is established.

RULE 5.9-2:
If a module implements the MSIB link remote capability, the **LINK REMOTE** MSIB command **MUST** put the link in the remote state and disable manual control of the instrument.

RULE 5.9-3:
If a module implements the MSIB link remote capability, the **LINK LOCAL** MSIB command **MUST** put the link in the local state.

PERMISSION 5.9-4:
If the MSIB link remote capability is not implemented, the link **MAY** be designed to be in either the local or remote state when the link is established.

SUGGESTION 5.9-5:
If the MSIB link remote capability is not implemented, it is preferable for the link to be in the local state when it is established.

OBSERVATION 5.9-6:
The MSIB link remote capability is an optional capability.

5.10 Status Message

A status message is associated with a link initiator or a link responder as defined by particular link types. The status message can be sent when a condition becomes true or on request.

RULE 5.10-1:
The **STATUS** and **SEND STATUS** MSIB commands **MUST** only be applied to the currently selected data stream.

RULE 5.10-2:
When the condition is true that a logical module would generate a service request, it **MUST** use the **STATUS** MSIB command to provide its status message to its control link initiator.

5.10.1 Status Message for Control Links

RECOMMENDATION 5.10.1-1:
The definition of a logical module's status message should be the same on its control link as its IEEE 488.1 interface definition.

5.11 Module Addressing

A module's address is an 8-bit value with 256 unique settings. The low order 5-bits are used to set the column address and the upper 3-bits are used to set the row address. Addresses are referred to as a pair: row, column. It is useful to view the address range as shown in figure 5-5.

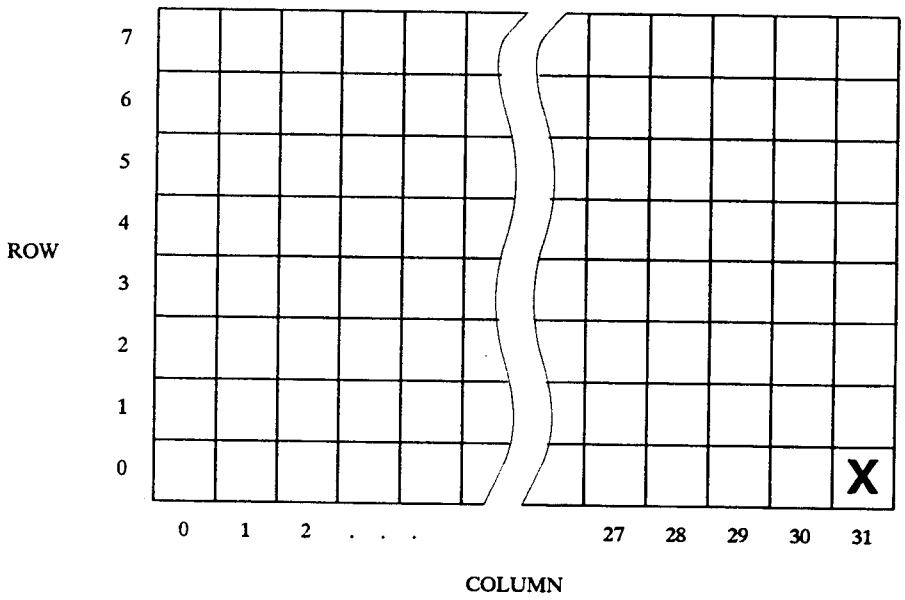


Figure 5-5. Address Map

5.11.1 Setting Module Address

RECOMMENDATION 5.11.1-1:

The column address entry should also be used for the IEEE 488.1 address in order to simplify address entry.

RULE 5.11.1-2:

A logical module **MUST** provide a non-volatile means to set its 8-bit address without communicating over either the IEEE-488.1 or MSIB.

SUGGESTION 5.11.1-3:

A convenient way to set a module's address is by providing an 8-position dip switch, on the rear panel of a module, to enter the row and column addresses. The most significant bit of the row address should be the most left switch and the least significant bit of the column address should be the most right switch.

RULE 5.11.1-4:
Address 0, 31 **MUST NOT** be used as a valid address setting. Address 0, 31 is used for testing purposes as an address that is known to have no module.

OBSERVATION 5.11.1-5:
A column address of 31, which is also the IEEE 488.1 address, is also not legal on IEEE 488.1.

5.11.2 Soft Address

There are circumstances where it is advantageous to set the IEEE 488.1 address remotely by the use of an MSIB command.

RULE 5.11.2-1:
A module with both an IEEE 488.1 interface and an MSIB interface **MUST** immediately respond to the **SET IEEE 488.1 ADDRESS** MSIB command to allow the user to change the module's IEEE 488.1 address.

SUGGESTION 5.11.2-2:
A soft address setting is most useful if a module stores its soft IEEE 488.1 address in non-volatile memory so that the address will be remembered through a power cycle.

PERMISSION 5.11.2-3:
A module without non-volatile storage capability **MAY** be designed so that a soft IEEE 488.1 address reverts to its no volatile value when power goes away.

RULE 5.11.2-4:
A module **MUST** have a means to override the soft set address.

SUGGESTION 5.11.2-5:
As a means to manually change the soft set IEEE 488.1 address, a module at power-on should check the address switches against what they were the last time the soft address was set. If they are different, then the module should use the switch value.

5.11.3 Row Zero Address Relationships

A row value of 0 is used by instruments and modules which provide graphics links to locate each other without a complete address search.

RECOMMENDATION 5.11.3-1:
Instrument systems should be planned with user controllable instruments located on row 0 so that modules which provide keyboard and graphics links can provide easy access to the instruments.

RECOMMENDATION 5.11.3-2:
Modules which provide graphics and keyboard links should be designed to take advantage of row 0 to provide quick location of instruments for manual control.

RECOMMENDATION 5.11.3-3:
Modules which provide graphics links should be placed on row 0 to provide system error reporting functions.

5.11.4 Master Slave Address Relationships at Power-On

A module's address determines relationships between modules thereby allowing the system to configure multiple module instruments at power-on. The master module controls the functions of its slave modules to provide measurement functionality. The master module provides the interface to the multiple module instrument through IEEE 488.1 and MSIB remote interfaces as well as graphics and keyboard links. Multiple module instruments may also be slaves to other masters as a component of another multiple module instrument.

RECOMMENDATION 5.11.4-1:
When there is a module which needs to control one or more modules via control links, the master slave address relationship should be used to define power-on configuration.

PERMISSION 5.11.4-2:
In cases where the master slave address relationship will not serve the system configuration needs, other module specific algorithms **MAY** be used to define the relationship between modules.

5.11.4.1 Power-On Slave Space Definition
The slave space of a master module is viewed as a rectangular area with cut out sections that allow for the slave space of other masters within that space as shown in figure 5-6.

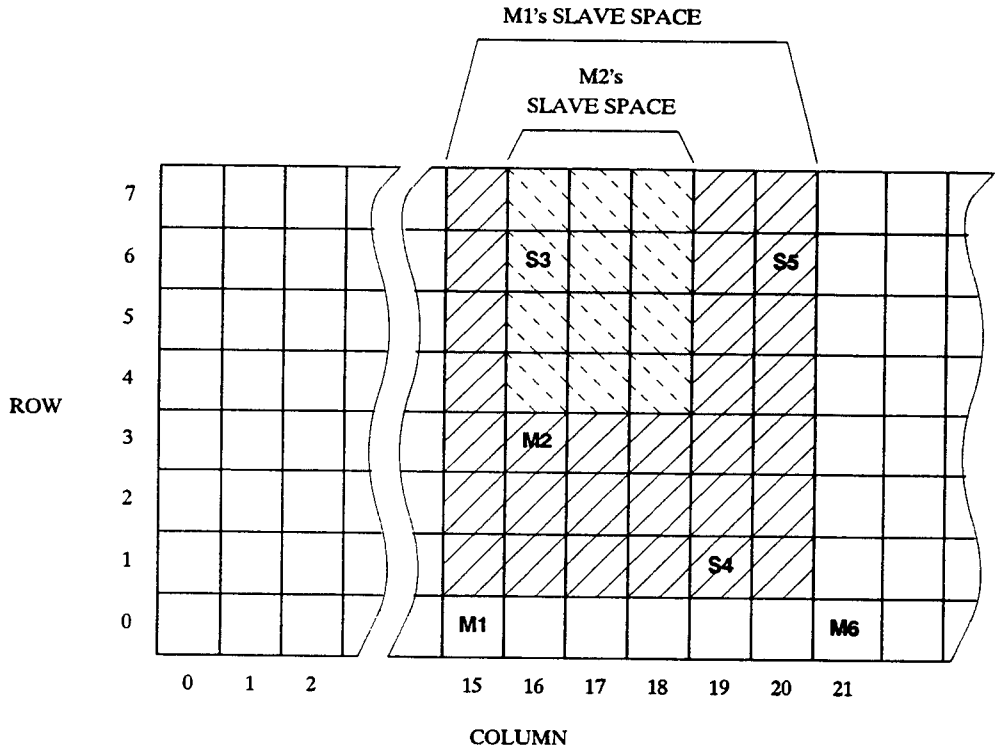


Figure 5-6. Master Module Slave Space

- The lowest row of a master's slave space is the row immediately above the master module.
- The highest row of a master's slave space is the highest row of the MSIB address which is row 7.
- The lowest column of a master's slave space is the column equal to the master's column address.
- The highest column of a master's slave space is the lower of: the highest column address (31) or the column at or above the master's column address that is less than the column address where another module resides that has a row address equal to or less than the master.
- The slave area of other masters is excluded from a master's slave area.

SUGGESTION 5.11.4.1-1:

A master can test for the presence of other modules by sending the **NULL** MSIB command. It can be determined from the MSIB interface if a module is present when attempting to transmit a packet.

RULE 5.11.4.1-2:

A master module **MUST** determine if a module is another master module by sending the **SEND MODULE ID** MSIB command.

5.12 Initialization

After power is applied to a mainframe, its MSIB system will become ready when all other mainframes are powered on and are able to communicate over MSIB. When the MSIB system becomes ready, modules then initialize and run self tests. This is followed by master modules determining their slave modules and then setting themselves up in the power-on measurement state.

RULE 5.12-1:
A module **MUST** determine when the MSIB system is ready by sending the **NULL** MSIB command to Address 0, 31 and waiting for the interface to respond that the transmission is complete.

RULE 5.12-2:
The module **MUST** blink its error light at a rate of approximately 1 Hz (50% duty cycle) when the MSIB interface is not ready.

RULE 5.12-3:
A module's MSIB interface **MUST** be initialized and ready to receive packets within 700 ms after the MSIB system is ready.

PERMISSION 5.12-4:
A module **MAY** continue to initialize itself after initializing its MSIB interface, thus holding off the first MSIB packet until it is fully initialized.

RULE 5.12-5:
A module **MUST NOT** send packets to any other module until one second after the MSIB system is functional.

PERMISSION 5.12-6:
A module **MAY** send packets to itself or MSIB address 0, 31 at any time after it has initialized its own interface.

RULE 5.12-7:
A module **MUST NOT** at any time prior to, during, or after its initialization of the MSIB appear at any address other than its assigned address.

RECOMMENDATION 5.12-8:
A module self test should be run as a part of the power-on initialization sequence.

5.13 Self Test

5.13.1 MSIB Self Test

RULE 5.13.1-1:
A minimum MSIB self test **MUST** consist of the following:

- Send the **NULL** MSIB command to address 0, 31. Since it is illegal for a module to reside at this address, the MSIB interface should indicate that there is no module at this address.
- Send one or more data or command packets on the module's own address and verify the data. This will verify that packets can be sent without corrupting their contents.

RULE 5.13.1-2:
If a failure on the MSIB interface is detected, the module **MUST** blink its error indicator at a rate of approximately 1 Hz (50% duty cycle) until the interface is operating properly. The error light **MUST NOT** blink in this manner when the MSIB interface is ready and operating properly.

5.13.2 Module Self Test

RECOMMENDATION 5.13.2-1:
During module self test, all of the module's front panel indicators should be illuminated.

RECOMMENDATION 5.13.2-2:
Errors determined during module self test should be reported using the module's error handling mechanism that is used during normal module operation.

RECOMMENDATION 5.13.2-3:
A module's self test should complete within 10 seconds.

5.14 Busy Bus Test Mode

The busy bus test mode is used during evaluation of electromagnetic compatibility testing of modules. This defines a method of generating constant bus activity for evaluation purposes.

SUGGESTION 5.14-1:
A module should have a method for generating a constant re-transmission of a packet over MSIB.

OBSERVATION 5.14-2:
An easy way to generate constant re-transmission of an MSIB packet is to send a packet to your own address while not reading the transmitted packet. After sending enough packets to fill the modules own hardware input buffer, the module will begin indicating a busy condition. This causes the transmitter section of the MSIB interface to constantly re-transmit the packet.

SUGGESTION 5.14-3:
A method to indicate for the module to power up in busy bus mode is to set the address to row 0, column 31. This is an illegal address for the system. The module is not allowed to set its address to this value, so it must power up at some other pre-defined address and begin the busy bus test.

RECOMMENDATION 5.14-4:
If a module powers up in the busy bus mode and the address is not selectable, it should power up at row 1, column 0.

OBSERVATION 5.14-5:
Only one module at a time should be used in busy bus test mode. Using busy bus mode **MAY** inhibit some system functions.

OBSERVATION 5.14-6:
A module generating a busy bus condition will not communicate with any other module. Therefore, it is important to enter this mode prior to the initialization requirement of rule 5.12-3.

5.15 Error Handling

When an error occurs in a logical module, the user is informed with error indicators on the logical module and any system error reporting modules. The user can inquire about the complete error report by either remote control or from any system error reporting modules.

RULE 5.15-1:
All logical modules **MUST** provide an error indicator on their front panel.

RULE 5.15-2:
A logical module's front panel error indicator **MUST NOT** be used for any other purpose other than defined by this specification.

RULE 5.15-3:
A logical module **MUST** light its error indicator when an error occurs. It **MUST** also extinguish its error indicator when all error conditions are cleared and all errors have been reported.

5.15.1 Module Error Indication

RULE 5.15.1-1:
When the error status of a module goes from no errors to one or more errors occurred and the module is on row zero, it **MUST** send the **ERROR OCCURRED** MSIB command to all other row zero modules.

RULE 5.15.1-2:
When all errors have been cleared and the errors have been reported and the module is on row zero, it **MUST** send the **ALL ERRORS CLEARED** MSIB command to all other row zero modules.

RULE 5.15.1-3:
A module which is the responder to a control link **MUST** keep the link initiator informed of its error status.

OBSERVATION 5.15.1-4:
If a module has any errors at the time a control link is established, it is important for the link responder to report this condition to the link intiator. Otherwise, the initiator of the control link will not be aware of the module's error status.

RULE 5.15.1-5:
A module which is the responder to a control link **MUST** use the **ERROR OCCURRED** MSIB command to inform the link initiator when the error status goes from no errors to one or more errors occurred. The module **MUST** also use the **ALL ERRORS CLEARED** MSIB command to report when all errors have been cleared and the errors have been reported.

PERMISSION 5.15.1-6:
For backwards compatibility a module may use a device dependent method to keep its control link initiator informed of its error status.

RULE 5.15.1-7:
A module that is not capable of directly reporting errors to the user **MUST** ignore an **ERROR OCCURRED** MSIB command and **ALL ERRORS CLEARED** MSIB command from modules which are not its slaves as they are intended for system error reporting modules.

5.15.2 System Error Reporting

RULE 5.15.2-1:
A system error reporting module **MUST** provide a facility to alert the user of errors that have been reported to it with the **ERROR OCCURRED** MSIB command regardless of whether or not modules have a link with the system error reporting module.

RULE 5.15.2-2:
A system error reporting module **MUST NOT** extinguish its indication of an error in the system until it receives the **ALL ERRORS CLEARED** MSIB command from all modules which sent an **ERROR OCCURRED** MSIB command.

RECOMMENDATION 5.15.2-3:
A system error reporting module determining an error within itself should use the same error reporting facilities used for module error reporting.

RULE 5.15.2-4:
When requested by a user, a system error reporting module **MUST** use the **SEND ALL ERRORS** MSIB command to acquire errors and then display those errors.

RULE 5.15.2-5:
A logical module **MUST** only consider an error reported if the detailed error description has been output with the **SEND ALL ERRORS** MSIB command or output from any one of its remote control interfaces.

5.16 Active Indicator

The purpose of the active indicator is to provide physical identification of a logical module. An example where the active indicator might be used, is the identifying of a particular module address on screen to a physical module.

RULE 5.16-1:
All logical modules **MUST** provide an active indicator on their front panel.

RULE 5.16-2:
A logical module's front panel active indicator **MUST NOT** be used for any purpose other than defined for this specification.

RULE 5.16-3:
The active indicator **MUST** be illuminated as instructed by the **LIGHT ACTIVE** and the **EXTINGUISH ACTIVE** MSIB commands.

RULE 5.16-4:
Each module **MUST** maintain a count of the number of **LIGHT ACTIVE** MSIB commands minus the number of **EXTINGUISH ACTIVE** MSIB commands received. The module's active indicator **MUST** be illuminated if and only if this count is greater than zero.

RULE 5.16-5:
A logical module **MUST** respond to the **LIGHT ACTIVE** and **EXTINGUISH ACTIVE** MSIB commands regardless of their source.

RULE 5.16-6:
For all modules that a logical module is controlling that are currently in use, a logical module **MUST** send the **LIGHT ACTIVE** and **EXTINGUISH ACTIVE** MSIB commands to keep those module's active indicators in the same state as its own active indicator.

PERMISSION 5.16-7:
A logical module **MAY** not activate the active indicators of modules it is controlling that are not in use.

RULE 5.16-8:
A **LIGHT ACTIVE** or **EXTINGUISH ACTIVE** MSIB command **MUST NOT** be sent in other than the following situations: when a keyboard link is established, a master module updating its slave module active light status, or a module identifying another module to the user.

OBSERVATION 5.16-9:
When an instrument is manually operated, all of the modules used to make the measurement will be identified with their active indicators.

5.17 Module Message Indication

A module message indication may be used when an indication is needed and the normal communication mechanisms are not available. An example of this condition is a module that is unable to communicate a message because its MSIB interface is busy waiting for another module to respond.

PERMISSION 5.17-1:
A logical module **MAY** indicate a module specific message by blinking its error and active indicators synchronously at a rate of 1 Hz (50 % duty cycle).

5.18 MSIB Commands

An MSIB command is a 16-bit message sent over MSIB as a single packet with the command bit set to true.

TABLE 5-5. MSIB Commands

Value	Mnemonic	Purpose	Rev
0000H	NULL	No operation	1.0
0001H	END	Terminate message (like IEEE 488.1 END)	1.0
0002H	SEND CAPABILITY	Request module's capabilities	2.0
0003H	RESERVED	No operation, must accept	1.0
0004H	RESERVED	No operation, must accept	1.0
0005H	RESERVED	No operation, must accept	1.0
0006H	RETURN TO LOCAL	Same as IEEE 488.1 rtl	1.0
0007H	LOCK LINK	Lock a link	1.0
0008H	UNLOCK LINK	Unlock a link	1.0
0009H	LIGHT ACTIVE	Light active annunciator	1.0
000AH	EXTINGUISH ACTIVE	Turn off active annunciator	1.0
000BH	ERROR OCCURRED	Signal an error has occurred	1.0
000CH	ALL ERRORS CLEARED	Signal no errors are present	1.0
000DH	UNRECOGNIZED COMMAND	MSIB command not recognized	1.0
000EH	ILLEGAL COMMUNICATION	Signal protocol violation	1.0
0010H	SEND STATUS	Request status message	1.0
0011H	SEND ALL ERRORS	Request error message strings	1.0
0012H	SEND MODULE ID	Request module ID string	1.0
0013H	SEND MANUFACTURER ID	Request identity of manufacturer	2.0
0014H	SEND TIME	Request time	2.0
0015H	LINK REMOTE	Place link in remote state	2.0
0016H	LINK LOCAL	Place link in local state	2.0
0017H	SEND MODEL NUMBER	Request module's model number	2.1
0018H	SEND SERIAL NUMBER	Request module's serial number	2.1
0019H	SEND FIRMWARE REVISION	Request module's firmware revision	2.1
001AH	TRANSMIT OFF	Do not transmit to the selected link	2.2
001BH	TRANSMIT ON	OK to transmit to the selected link	2.2
01xxH	ESTABLISH NON-TAGGED LINK	Establish non-tagged link	1.0
02xxH	BREAK LINK	Break tagged or non-tagged link	1.0
03xxH	ACCEPT LINK	Accept tagged or non-tagged link	1.0
04xxH	REJECT LINK	Reject tagged or non-tagged link	1.0
05xxH	ACCEPT BREAK LINK	Accept break tagged or non-tagged link	1.0
06xxH	STATUS	Return status byte or request service	1.0
07xxH	SET IEEE 488.1 ADDRESS	Set soft IEEE 488.1 address	1.0
08xxH	COMMAND RESPONSE	Respond to MSIB request	1.0
0900H	END COMMAND RESPONSE	Terminate MSIB response	1.0
0AxxH	IDENTIFY LINK INITIATOR	Identify tagged link initiator	2.0
0BxxH	IDENTIFY LINK RESPONDER	Identify tagged link responder	2.0
0CxxH	SELECT LINK	Select tagged link for subsequent data	2.0
0ExxH	ESTABLISH TAGGED LINK	Establish tagged link	2.0

RECOMMENDATION 5.18-1:
Logical modules should implement the most recent revision of the Modular Measurement System communication protocol specification.

RULE 5.18-2:
An MSIB command **MUST** be sent with the CMD bit true.

RULE 5.18-3:
Every command **MUST** be implemented as indicated by the requirement section of the description of the command.

NULL: (0000H) -- This command means do nothing and is used for testing the MSIB. It is often used to test for the presence of a module.

Sender: There are no restrictions.

Receiver: No action is taken.

Requirement: Required for all modules by *Protocol Revision 1.0.*

END: (0001H) -- This command indicates the end of data. **END** is also defined in the context of the language used to communicate over a link. All transmissions must be terminated by **END** MSIB command to guarantee their execution.

Sender: Used to terminate all transmissions. It is best to terminate at the smallest syntactical element allowed by the language used over the link.

Receiver: End of data has been reached. It is permissible for the receiver of a message to wait until an **END** MSIB command is received before processing a transmission.

Requirement: Required to be recognized by *Protocol Revision 1.0.*
Required to guarantee execution by *Protocol Revision 2.1.*

SEND CAPABILITY: (0002H) -- Inquire as to a module's capability. The capability is returned as a string of bytes (maximum length 128 bytes) with capabilities represented by bits or groups of bits. Capability bits will be assigned from the least to the most significant bits of a byte and from the first to the last byte of the string. If a module receives a capability string with fewer bytes than it expects, it should assume the bytes it did not receive are all zeros. The sending module does not support the capabilities represented by the bits in the missing bytes. If a module receives a capability string with more bytes than it expects, it should discard the excess bytes and only use the bytes it knows about. The sending module supports (or has the definition for) more capabilities than the receiving module knows about. In this case the receiving module simply ignores the excess capabilities.

The capability string is to be returned using the **COMMAND RESPONSE** and **END COMMAND RESPONSE** commands.

The capabilities currently defined for **SEND CAPABILITY** are:

Byte	Bit	Definition
1	0	Keyboard responder - module will accept keyboard link
1	1	Graphics responder - module will accept graphics link
1	2	Control responder - module will accept control link
1	3	Storage responder - module will accept storage link
1	4	Tagged links - module supports tagged links
1	5	Master - module has a slave space
1	6	Time - module responds to time query
1	7	MSIB Remote - module supports MSIB remote/local
2	0	IEEE 488.1 - module has an IEEE 488.1 interface
2	1	Responds to **TRANSMIT ON** and **TRANSMIT OFF**

Sender: Send this command to determine a module's capabilities.

Receiver: Return capability string as described above. This response must be the same every time during operation. It may change after a system reset.

Requirement: Required for all modules by *Protocol Revision 2.0.*

RESERVED: (0003H, 0004H, 0005H) -- This command has no operation associated with it. It is reserved for compatibility with modules prior to the issue of this specification.

Sender: Not for new design.

Receiver: This command must be accepted with no operation resulting.

Requirement: Required for all modules by *Protocol Revision 1.0.*

RETURN TO LOCAL: (0006H) -- Performs same actions as IEEE 488.1 rtl.

Sender: Sent to put a module into a local state with respect to its IEEE-488.1 interface.

Receiver: The command sends an rtl message to the IEEE 488.1 interface as per IEEE 488.1. If an IEEE 488.1 interface is not present, then this command is ignored.

Requirement: Required for all modules by *Protocol Revision 1.0.*

LOCK LINK: (0007H) -- This command is used by a link initiator to prevent the responder from being taken away by another module. Sending this command prevents the responder from breaking the link unless there is an illegal communication detected from that address.

Sender: Link initiator sends this command to Link Responder.

Receiver: If a command comes from the initiator of a link, then put that link into the locked state, otherwise an **ILLEGAL COMMUNICATION** must be reported.

Requirement: Required for all modules by *Protocol Revision 1.0.*

UNLOCK LINK: (0008H) -- This command is used by a link initiator to allow the responder to break the link if necessary.

Sender: Link initiator sends to Link Responder.

Receiver: If a command comes from the initiator of a link, then put that link into the unlocked state, otherwise an **ILLEGAL COMMUNICATION** must be reported.

Requirement: Required for all modules by *Protocol Revision 1.0.*

LIGHT ACTIVE: (0009) -- The active annunciator on the front panel is lit by this command. A count of **LIGHT ACTIVE** commands received is maintained.

Sender: The **LIGHT ACTIVE** MSIB command is sent to a module to identify its physical location. A module receiving the **LIGHT ACTIVE** MSIB command from a link initiator will also send the **LIGHT ACTIVE** MSIB command to its slave modules that are currently in use.

Receiver: Increment light active count. Light ACTIVE annunciator if it is not already on. If command came from a link initiator, send to all active slaves.

Requirement: Required for all modules by *Protocol Revision 1.0.*

EXTINGUISH ACTIVE: (000AH) -- Extinguish the active annunciator on the front panel.

Sender: The **EXTINGUISH ACTIVE** MSIB command is sent whenever the sender no longer wants to physically identify the module.

Receiver: Decrement light active count. If count becomes zero, turn off ACTIVE annunciator. If command came from a link initiator, send to all active slaves.

Requirement: Required for all modules by *Protocol Revision 1.0.*

ERROR OCCURRED: (000BH) -- This command signifies that an error has occurred in the sending module.

Sender: If there is a control responder link, the module sends this command to the Link initiator. If on row zero, the module broadcasts this command to all other row-zero addresses.

Receiver: Devices capable of directly reporting errors: Update their error indicator. Control Link Initiator: Go read error(s) from module. Others : Ignore.

Requirement: Required for all modules by *Protocol Revision 1.0.*

ALL ERRORS CLEARED: (000CH) -- This command signifies that the sending module does not have any reportable errors.

Sender: If there is a control responder link, the module sends this command to the Link initiator. If on row zero, the module broadcasts this command to all other row-zero addresses.

Receiver: Devices capable of directly reporting errors: Update their error indicator. Control Link Initiator: Module errors cleared. Others : Ignore.

Requirement: Required for all modules by *Protocol Revision 1.0.*

UNRECOGNIZED COMMAND: (000DH) -- The sender did not recognize an MSIB command sent by the receiver.

Sender: Send to the source module of a received unrecognized MSIB command. Do **NOT** report an error.

Receiver: The sender did not recognize one of the MSIB commands that was sent. If this situation is not expected, then report an error.

Requirement: Required for all modules by *Protocol Revision 1.0.*

ILLEGAL COMMUNICATION: (000EH) -- This command is sent when any message is received that is not legal at this time. The module which receives this MSIB command must reset to an idle state all links with the module which sent the command.

Sender: Send to source module of received illegal message. An error should be reported. Immediately reset all links with the receiver.

Receiver: Immediately reset all links with sender to an idle state.

Requirement: Required for all modules by *Protocol Revision 1.0.*

SEND STATUS: (0010H) -- Request module status byte; response is the **STATUS** MSIB command.

Sender: Requests status byte from a module for the currently selected link.

Receiver: Respond with the **STATUS** MSIB command. Lower byte contains status byte. This is a part of the currently selected link.

Requirement: Required for all modules by *Protocol Revision 1.0.*

SEND ALL ERRORS: (0011H) -- This is a request for an error description; response is text that can utilize up to twenty lines on a system error reporting module. The text is ASCII characters with carriage return and line feed to separate each line. Each line is a maximum of 50 characters. Each character is the lower byte of an **COMMAND RESPONSE** packet. The **END COMMAND RESPONSE** is sent as a terminator. Only an **END COMMAND RESPONSE** should be sent if no errors exist. It is recommended that an error number precede text when errors exist.

Sender: Used to request error text from any module.

Receiver: Respond with error text within a series of **COMMAND RESPONSE** packets which is terminated with **END COMMAND RESPONSE.**

Requirement: Required for all modules by *Protocol Revision 1.0.*

SEND MODULE ID: (0012H) -- A request for identification of a module is initiated with this command. The response will consist of at least four items separated by commas. The maximum number of characters is 128. The items are:

1. A model number of up to seven characters.
2. A module identification string.
3. One character encoding for a master module (M) compared to a non-master module (N).
4. Two characters which are either the IEEE 488.1 address or, if IEEE 488.1 is logically disabled, the characters **NO.**
5. A protocol revision number as an ASCII string representation of a floating point number with larger numbers meaning later revisions. Absence of this item indicates a *Protocol Revision of 1.0.*

All item response characters are ASCII in the range of 32 to 126 excluding comma and are sent as the lower byte of a series of **COMMAND RESPONSE** MSIB commands. This sequence of characters is terminated by the **END COMMAND RESPONSE** MSIB command and is used to identify modules

during instrument configuration. Example response strings are 70900A, LO/CONTROL, M, 18 and 99999A, MYTHICAL, N, NO, 2.

Sender: Used to request module ID text from any module.

Receiver: Respond with the module ID text within a series of **COMMAND RESPONSE** packets terminated with **END COMMAND RESPONSE.**

Requirement: Required for all modules by *Protocol Revision 1.0.*

SEND MANUFACTURER ID: (0013H) -- Request the identity of a module's manufacturer. The manufacturer ID is returned as a string of ASCII characters in the range 32 to 126 (maximum length 128 characters). The list of manufacturers' identification strings is available on request from the MMS consortium. The manufacturer ID string is to be returned using the **COMMAND RESPONSE** and **END COMMAND RESPONSE** commands.

Sender: Send this command to request the identity of a module's manufacturer.

Receiver: Return manufacturer ID as described above.

Requirement: Required for all modules by *Protocol Revision 2.0.*

SEND TIME: (0014H) -- This command requests the current time. The current time is sent in the following format:

Y Y Y Y M M D D h h m m s s f f f f f f <end>

Where:

Y Y Y Y	=	Year
M M	=	Month (1 . . 12)
D D	=	Day (1 . . 31)
h h	=	hour (00 . . 23)
m m	=	minute (0 . . 59)
s s	=	second (0 . . 59)
f f f f f f	=	fraction of a second
<end>	=	**END COMMAND RESPONSE**

If the date is not available, then the date fields (Y Y Y Y M M D D) are all zeros. The "fraction of a second" field is optional and may contain any number of digits. If the time is invalid or not available, the response is <end> with no other data.

The time is to be returned using the **COMMAND RESPONSE** and **END COMMAND RESPONSE** commands.

Sender: Send this command to determine the current date and time.

Receiver: If the current time is known, return in the format described above.

Requirement: Required by *Protocol Revision 2.0* if time is supported.

LINK REMOTE: (0015H) -- The sending module is putting this link into the remote state. Once in remote state, if a keyboard link is active, the menu key labels will be blanked and key presses will be

ignored.

Sender: Send this command to place the receiver in remote.

Receiver: If a link is established set this link to remote, blank the menu key labels and ignore key presses. If there is no link, an **ILLEGAL COMMUNICATION** must be reported.

Requirement: Required by *Protocol Revision 2.0* if module supports MSIB remote/local.

LINK LOCAL: (0016H) -- The sending module is putting this link into the local state. If no other links are in the remote state and a keyboard link is active, the menu key labels will be restored and key presses will once again be processed.

Sender: Send this command to return the receiver to local.

Receiver: If a link is established, return this link to local. If no other links are in remote then restore the menu key labels and resume processing key presses. If there is no link, an **ILLEGAL COMMUNICATION** must be reported.

Requirement: Required by *Protocol Revision 2.0* if module supports MSIB remote/local.

SEND MODEL NUMBER: (0017H) -- Request for a module's model number. The module model number is returned as a string of ASCII characters in the range 32 to 126 (maximum length 128 characters). The module model number is to be returned using the **COMMAND RESPONSE** and **END COMMAND RESPONSE** commands.

Sender: Send this command to request a module's model number.

Receiver: Return model number as described above.

Requirement: Required for all modules by *Protocol Revision 2.1.*

SEND SERIAL NUMBER: (0018H) -- Request for a module's serial number. The module serial number is returned as a string of ASCII characters in the range 32 to 126 (maximum length 128 characters). The module serial number is to be returned using the **COMMAND RESPONSE** and **END COMMAND RESPONSE** commands.

Sender: Send this command to request a module's serial number.

Receiver: Return serial number as described above.

Requirement: Required for all modules by *Protocol Revision 2.1.*

SEND FIRMWARE REVISION: (0019H) -- Request for a module's firmware revision. The module firmware revision is returned as a string of ASCII characters in the range 32 to 126 (maximum length 128 characters).

The module firmware revision is to be returned using the **COMMAND RESPONSE** and **END COMMAND RESPONSE** commands.

Sender: Send this command to request a module's firmware revision.

Receiver: Return firmware revision as described above.

Requirement: Required for all modules by *Protocol Revision 2.1.*

TRANSMIT OFF: (001AH) -- This command is used to disable another module from transmitting link specific packets to the currently selected tagged link.

Sender: A module sends this command when it needs to stop another module from sending data on a tagged link. To determine when the other module has stopped sending packets on this link, send two **NULL** MSIB commands following the **TRANSMIT OFF**. After the second **NULL** is accepted, no further packets will be sent on this link.

Receiver: When this command is received the module must stop sending data to this tagged link until a **TRANSMIT ON** MSIB command is received. Take no additional packets from this link until it can be guaranteed that no packets will be sent on this link.

Requirement: Required by *Protocol Revision 2.2* if module supports transmit pacing.

TRANSMIT ON: (001BH) -- This command is used to enable another module to transmit to the currently selected tagged link.

Sender: A module uses this command when it needs to enable output from another module on a tagged link.

Receiver: When this command is received the module must resume sending available data to this tagged link.

Requirement: Required by *Protocol Revision 2.2* if module supports transmit pacing.

ESTABLISH NON-TAGGED LINK: (010xH) -- The sending module wishes to establish a non-tagged link with the receiving module. The type of link being established is defined by the lower byte of this command. The non-tagged link types are as follows:

TABLE 5-6. Link Types for Non-Tagged Links

0	Keyboard link
1	Graphics link
2	Control link

Sender: Send this command to establish a non-tagged link with another module.

Receiver: Respond with either **ACCEPT LINK** or **REJECT LINK** as appropriate.

Requirement: Required for all modules by *Protocol Revision 1.0.*

BREAK LINK: (020xH) -- The sending module wishes to break a link currently established with the receiving module. The receiving module has no choice but to accept the break. The type of link is defined by the lower byte of this command.

Sender: Send this to a module to break a link. No more data may be sent following this command.

Receiver: There is no choice but to respond with **ACCEPT BREAK LINK**. Any pending function should be terminated to allow the **ACCEPT BREAK LINK** to occur as soon as possible. Data may be sent before the **ACCEPT BREAK LINK** command, but no replies will be received. If a **BREAK LINK** command has been sent to the module from which this command is received, then this command is to be treated as the accept. If this command is received from a module with which there is no link established then an **ILLEGAL COMMUNICATION** must be reported.

Requirement: Required for all modules by *Protocol Revision 1.0.*

ACCEPT LINK: (030xH) -- The sending module is willing to accept the link requested by the receiving module. The type of link is defined by the lower byte of this command.

Sender: Send this command to accept a link. If the link being accepted is a tagged link then also send the **IDENTIFY LINK RESPONDER.**
Data communication may now begin.

Receiver: The link has been accepted. If the link is a tagged link then respond with **IDENTIFY LINK INITIATOR.** Data communication may now begin. If this command is received from a module to which an **ESTABLISH NON-TAGGED LINK** or **ESTABLISH TAGGED LINK** command has not been sent then an **ILLEGAL COMMUNICATION** must be reported.

Requirement: Required for all modules by *Protocol Revision 1.0.*

REJECT LINK: (040xH) -- The sending module is not willing to accept the link requested by the receiving module. The type of link is defined by the lower byte of this command.

Sender: Send this command to reject a link.

Receiver: The link has been rejected. No data communication may take place. If this command is received from a module to which an **ESTABLISH NON-TAGGED LINK** or **ESTABLISH TAGGED LINK** command has not been sent then an **ILLEGAL COMMUNICATION** must be reported.

Requirement: Required for all modules by *Protocol Revision 1.0.*

ACCEPT BREAK LINK: (050xH) -- The sending module is accepting the break of a link with the receiving module. The type of link is defined by the lower byte of this command.

Sender: Send in response to **BREAK LINK.** No data may be sent following this command.

Receiver: The sending module has accepted the break. The link is now broken. If this command is received from a module to which a **BREAK LINK** command has not been sent then an **ILLEGAL COMMUNICATION** must be reported.

Requirement: Required for all modules by *Protocol Revision 1.0.*

STATUS: (06xxH) -- This command contains an eight bit status byte as the second data byte of the packet. This command provides both the request for service and the status byte information.

Sender: Reports status immediately for the currently selected link.

Receiver: Status is either in response to **SEND STATUS** or is a request for service. This is a part of the currently selected link.

Requirement: Required for all modules by *Protocol Revision 1.0.*

SET IEEE 488.1 ADDRESS: (07xxH) -- This command sets the IEEE 488.1 address of the receiving module with an IEEE 488.1 interface. The lower byte of this command is new IEEE 488.1 address. If the new address indicated is 31 or greater, the IEEE 488.1 address will be set to the value currently set on the module's address switches.

Sender: Send to a row-zero address module to change its IEEE 488.1 address. In Protocol Revision-1.0 it can be determined if a module has an IEEE 488.1 interface by the **SEND MODULE ID** MSIB command.

Receiver: Used to alter the soft settable IEEE 488.1 address.

Requirement: Required by *Protocol Revision 1.0* if module has IEEE 488.1 Interface.

COMMAND RESPONSE: (08xxH) -- The lower byte of this command is a data byte being sent in response to another MSIB command.

Sender: Send with each byte of data of MSIB response. Terminate the message with **END COMMAND RESPONSE**.

Receiver: If this command is received other than in response to a command such as **SEND MODULE ID** then an **ILLEGAL COMMUNICATION** must be reported.

Requirement: Required for all modules by *Protocol Revision 1.0*.

END COMMAND RESPONSE: (0900H) -- This command terminates the response to an MSIB command.

Sender: Send this command as last byte of MSIB response message (see **COMMAND RESPONSE**).

Receiver: If this command is received other than in response to a command such as **SEND MODULE ID** then an **ILLEGAL COMMUNICATION** must be reported.

Requirement: Required for all modules by *Protocol Revision 1.0*.

IDENTIFY LINK INITIATOR: (0AxxH) -- This command is used by the initiator of a tagged link to identify the link being established. The lower byte of this command is the tag used by the responder to identify communications being sent to the initiator. The most significant four bits of the tag are chosen as a convenient value for the initiator. The least significant four bits are defined by the link type listed in table 5-7.

Sender: Send this command after receiving an **ACCEPT LINK** command that is in response to an **ESTABLISH TAGGED LINK** command.

Receiver: The tag in the lower byte of this command should be recorded and used to identify all communications to the initiator over this link.

Requirement: Required by *Protocol Revision 2.0* if tagged links are supported.

IDENTIFY LINK RESPONDER: (0BxxH) -- This command is used by the responder of a tagged link to identify the link being established. The lower byte of this command is the tag used by the initiator to identify communications being sent to the responder. The most significant four bits of the tag are chosen as a convenient value for the responder. The least significant four bits are defined by the link type as shown in table 5-7.

Sender: Send this command after sending an **ACCEPT LINK** command that is in response to an **ESTABLISH TAGGED LINK** command.

Receiver: The tag in the lower byte of this command should be recorded and used to identify all communications to the responder over this link.

Requirement: Required by *Protocol Revision 2.0* if tagged links are supported.

SELECT LINK: (0CxxH) -- This command is sent to a module to indicate which previously identified tagged link is being used to send all subsequent data.

Sender: Send this command whenever data being sent to a module is related to a different tagged link than the previous data sent to that module. The lower byte contains the tag that the receiving module previously indicated (by use of the **IDENTIFY LINK RESPONDER** and **IDENTIFY LINK INITIATOR** commands) should be used to identify this link.

Receiver: Subsequent data should be sent to the link indicated by the tag in the lower byte of this command.

Requirement: Required by *Protocol Revision 2.0* if tagged links are supported.

ESTABLISH TAGGED LINK: (0E0xH) -- The sending module wishes to establish a tagged link with the receiving module. The type of link being established is defined by the lower byte of this command. The tagged link types are as follows:

TABLE 5-7. Link Types for Tagged Links

0	Keyboard link
1	Graphics link
2	Control link
3	Storage link
4	Data link

Sender: Send this command to establish a tagged link with another module.

Receiver: Respond with either **ACCEPT LINK** or **REJECT LINK** as appropriate. If accepting the link also send **IDENTIFY LINK RESPONDER**.

Requirement: Required by *Protocol Revision 2.0* if tagged links are supported.

6. MECHANICAL INTERFACE

6.1 Module Specifications

6.1.1 Module Envelope/ Interface

RULE 6.1.1-1:
MMS modules **MUST** be designed according to the specifications given in figures 6-4 through 6-15.

OBSERVATION 6.1.1-2:
Figures 6-4 through 6-15 depict specifications for 1, 2, 3, and 4 slot modules. This in no way limits the width of a module to 4 slots. Width dimensions for modules greater than 4 slots can be calculated using the following formulas:

$$\text{Module Front Width} = (47.6 + (N\text{-}1) \times 48.39) \pm 0.2$$

$$\text{Module Rear Width} = (46.4 + (N\text{-}1) \times 48.39) \pm 0.4$$

where,

N = number of slots
dimensions are in mm

OBSERVATION 6.1.1-3:
Figures 6-2 and 6-3 give an overview of the principal module datums and their functions. These datums are used throughout figures 6-4 through 6-15.

RULE 6.1.1-4:
Every MMS module **MUST** use only one module latch assembly (items 1-3,12), figure 6-4.

OBSERVATION 6.1.1-5:
Having more than one module latch assembly per module can result in damage to either the module latch assembly (items 1-3,12), figure 6-4, or to the mainframe latch assembly (items 1,12,20-23), figure 6-47, during module installation or removal.

RULE 6.1.1-6:
Every MMS module **MUST** use a module primary rear bushing (item 10, Module Datum D), figure 6-8.

RECOMMENDATION 6.1.1-7:
Modules which have a width greater than 2 slots should incorporate a module secondary rear bushing (Module Datum J), figures 6-6 and 6-14.

OBSERVATION 6.1.1-8:
The module secondary rear bushing (Module Datum J), figures 6-6 and 6-14, helps to stabilize the module during shock and vibration. It also distributes forces to multiple mainframe guide pins (item 24, Mainframe Datum D), figure 6-31.

RULE 6.1.1-9:
Modules with multiple MSIB connectors (item 11), figure 6-25, **MUST** incorporate a module secondary rear bushing (Module Datum J), figures 6-6 and 6-14.

OBSERVATION 6.1.1-10:
The module secondary rear bushing (Module Datum J), figures 6-6 and 6-14, provides positional control for the mating of multiple MSIB connectors.

RULE 6.1.1-11:
Every MMS module **MUST** use only one module front alignment feature, figure 6-9. This module front alignment feature **MUST** be located on the same centerline as the module front location tab (Module Datum C), figure 6-4.

OBSERVATION 6.1.1-12:
The module front alignment feature, figure 6-9, is required to insure mating of the module front location tab (Module Datum C), figure 6-4, and the mainframe front location tab (Mainframe Datum C), figure 6-30. Use of more than one module front alignment feature can result in an interference fit between the additional module front alignment feature and it's corresponding mainframe latch assembly, (items 1,12,20-23), figure 6-47.

RULE 6.1.1-13:
Every MMS module **MUST** use a module rear alignment feature, figure 6-9. This module rear alignment feature **MUST** be located on the same centerline as the module primary rear bushing (item 10, Module Datum D), figure 6-8.

RECOMMENDATION 6.1.1-14:
The module rear alignment feature, figure 6-9, should be made out of plastic to avoid the potential for metal chipping or flaking as it slides down the mainframe channel, figure 6-35.

OBSERVATION 6.1.1-15:
The module rear alignment feature, figure 6-9, is required to insure mating of the module primary rear bushing (item 10, Module Datum D), figure 6-8, and the mainframe guide pin (item 24, Mainframe Datum D), figure 6-31.

RECOMMENDATION 6.1.1-16:
Every MMS module should use a module rear insertion feature, figure 6-9.

OBSERVATION 6.1.1-17:
The chamfered edges of the module rear insertion feature, figure 6-9, insure the smooth insertion of a module into a mainframe.

RULE 6.1.1-18:
The module rear location tab (Module Datum H), figure 6-9, **MUST** be located on the same centerline as the module primary rear bushing (item 10, Module Datum D), figure 6-8.

OBSERVATION 6.1.1-19:
The module primary rear bushing (item 10, Module Datum D), figure 6-8, provides the alignment needed for the module rear location tab (Module Datum H), figure 6-9, to engage the mainframe vibration stop (item 28), figure 6-37. This alignment will only be insured if the two module features are located on the same centerline.

SUGGESTION 6.1.1-20:
The module latch assembly (items 1-3,12), figure 6-4, should be located on the same centerline as the module MSIB connector (item 11), figure 6-25.

OBSERVATION 6.1.1-21:
The compression springs (item 9), figure 6-22, which provide float for the module MSIB connector (item 11), figure 6-25, can exert a 146 newton force when fully compressed. If the module latch screw is not in line with this force, torque will be introduced into the module.

PERMISSION 6.1.1-22:
The module front and rear access/extension areas, figure 6-8, **MAY** extend outside the z-axis envelope dimensions shown in figure 6-9.

OBSERVATION 6.1.1-23:
The module front and rear access/extension areas are accessible to the user when a module is fully engaged into a mainframe.

OBSERVATION 6.1.1-24:
A nominal 1.0 mm offset exists between Module Datum A (module front rear face) and Mainframe Datum A (mainframe front face) when the module is fully engaged into the mainframe as shown in figures 6-3 and 6-28.

RULE 6.1.1-25:
In a completely assembled module, the module MSIB connector (item 11), figure 6-25, **MUST** be allowed to rotate to the limit of its float range with a torque applied to the module connector indexing boss feature (module connector item 5) of 0.7 N-m or less.

6.1.2 Module MSIB Connector

RULE 6.1.2-1:
The module MSIB connector (item 11) **MUST** be designed according to the specifications given in figure 6-25. All dimensions apply after plating.

OBSERVATION 6.1.2-2:
Changing any dimensions relating to the module rear spring pin holes (Module Datum G), figure 6-5, connector bar (item 7), figure 6-21, spring pin (item 8), figure 6-23, compression spring (item 9), figure 6-22, or nut (item 6) could affect the x, y, or z-axes float of the module MSIB connector (item 11), figure 6-7. This float is required to allow for mainframe and module positional and length tolerances. The z-axis float also helps to prevent fretting corrosion, which can result from small relative movements between two rigidly mounted connectors.

OBSERVATION 6.1.2-3:
The shell (module connector item 1) of the module MSIB connector (item 11), figure 6-25, has a cutout which matches a corresponding feature on the module rear, figure 6-5. This insures that the module MSIB connector can be installed only one way, with the indexing boss feature correctly oriented.

RULE 6.1.2-4:
A second module MSIB connector (item 11), figure 6-25, **MUST** be used when module power exceeds 145 watts.

OBSERVATION 6.1.2-5:
The connector pin assignments for the module MSIB connector (item 11), figure 6-25, are shown in appendix A.1.

PERMISSION 6.1.2-6:
The module MSIB connector (item 11), figure 6-25, **MAY** have less than 50 socket contacts (module connector item 2) loaded.

RULE 6.1.2-7:
The mechanical durability of the module MSIB connector (item 11), figure 6-25, **MUST** be a minimum of 500 insertion/extraction cycles when measured per EIA STD RS-364-09.

RULE 6.1.2-8:
The insulation resistance of the module MSIB connector (item 11), figure 6-25, **MUST** be a minimum of 5000 MΩ at 500 VDC when measured per EIA STD RS-364-21A.

RULE 6.1.2-9:
The dielectric of the module MSIB connector (item 11), figure 6-25, **MUST** withstand 1500 VAC for 60 seconds when tested per EIA STD RS-364-20A Method A at sea level.

RULE 6.1.2-10:
The current rating of the module MSIB connector (item 11), figure 6-25, **MUST** be 3.0 amps per contact.

RULE 6.1.2-11:
The current resistance of the module MSIB connector (item 11), figure 6-25, **MUST** be 8.3 mΩ maximum per mated contact at rated current and temperature range.

RULE 6.1.2-12:
The module MSIB connector (item 11), figure 6-25, **MUST** be able to sustain continuous operation within a temperature range of -55° C to +95° C without a reduction in mechanical or electrical performance.

RULE 6.1.2-13:
The socket contacts (module connector item 2) of the module MSIB connector (item 11), figure 6-25, **MUST** be designed such that the module MSIB connector will have an insertion force while being mated to it's mainframe MSIB connector (item 29), figure 6-53, of not less than .139 newtons and not more than 1.39 newtons per contact, 67.6 newtons maximum for the mated connector pair.

RULE 6.1.2-14:
The socket contacts (module connector item 2) of the module MSIB connector (item 11), figure 6-25, **MUST** be designed and located such that each pin contact (mainframe connector item 5) of the mating mainframe MSIB connector (item 29), figure 6-53, is assured of electrical connection when entering anywhere within the thru hole diameter of the module MSIB connector static discharge shield (module connector item 6).

SUGGESTION 6.1.2-15:
Identification of socket contact positions (i.e. 1, 11, 22, 29, 40 and 50 as shown in figure 6-25) on the module MSIB connector can be helpful.

RECOMMENDATION 6.1.2-16:
Electrical continuity between the module MSIB connector static discharge shield (module connector item 6), figure 6-25, and the module MSIB connector shell (module connector item 1), figure 6-25, should be 10 Ω maximum.

OBSERVATION 6.1.2-17:
The static discharge shield (module connector item 6) of the module MSIB connector (item 11), figure 6-25, is part of the electrostatic discharge system of the connector which protects against possible damage caused by static discharge.

RULE 6.1.2-18:
The indexing boss feature (module connector item 5) of the module MSIB connector (item 11), figure 6-25, **MUST** be aligned as shown in figure 6-25 and held in position to within ± 2° with Module Connector Datum Y as reference.

RECOMMENDATION 6.1.2-19:
The material specifications for module connector items 1 through 6 should be as follows:

1. **Shell:** Zinc alloy; chromate conversion coat per MIL-C-5541.
2. **Socket Contact:** Beryllium copper per ASTM B196 alloy UNS No. C17300, temper TH04; gold plate .00076mm min. over .0013mm min. nickel plate; test per EIA STD RS-364-53.
3. **Socket Body:** 30% glass reinforced PET, PETRA 130 FR or RYTON R4 (P.P.S. per MIL-P-46174, Class 40).
4. **Securing Cap:** Aluminum alloy 6061-T6 per QQ-A-225/9; chromate conversion per MIL-C-5541.

5. **Indexing Boss:** Aluminum alloy 7075-T6 per QQ-A-225/9; electroless nickel plate per MIL-C-26074 Class I (0.0013-0.0025mm thk) over copper per MIL-C-15540.
6. **Static Discharge Shield:** CRES type 302 per QQ-S-766; passivate per QQ-P-35.

RULE 6.1.2-20:
The module MSIB connector (item 11), figure 6-25, **MUST** be able to withstand a torque applied to its indexing boss feature (module connector item 5) of 0.7 N-m. The module MSIB connector **MUST NOT** exhibit any reduction in its electrical or mechanical specifications after this torque has been applied.

6.1.3 Module Safety Grounding

RULE 6.1.3-1:
Each module **MUST** contain a low impedance, 20 mΩ maximum safety ground. The safety ground **MUST** work by contacting the mainframe guide pin (item 24, Mainframe Datum D), figure 6-31, as shown in figure 6-7. Each module **MUST** be designed so that this safety ground satisfies the requirements set forth in CSA Standard C-22.2, Number 0.4, *Bonding and Grounding of Electrical Equipment*, Paragraph 4.1.2.

OBSERVATION 6.1.3-2:
The module's safety ground connection to the mainframe at the mainframe guide pin (item 24, Mainframe Datum D), figure 6-31, serves two functions: a) it provides a path to the mainframe safety ground for fault currents, and b) it helps hold AC signal ground references to a common potential.

OBSERVATION 6.1.3-3:
The grounding spring (item 4), figure 6-20, shown in figure 6-7, is an example of a safety ground that has been used successfully.

OBSERVATION 6.1.3-4:
This is the only safety ground that is required between the module and the mainframe. Several types of shielding ground springs may be present on some mainframes. These springs are not required to be present on all mainframes and are not required to be designed as safety grounds.

OBSERVATION 6.1.3-5:
Neither Module Datum B/Mainframe Datum B alignment features, figures 6-4 and 6-29, nor the module/mainframe latch assemblies, figures 6-4 and 6-47, are reliable safety grounds. The electrical resistance of these interfaces depends on the torque applied to the latch screw (contact pressure).

6.1.4 Module EMC Grounding

RECOMMENDATION 6.1.4-1:
All module zones called out with Note 6.1.4-1 in figures 6-8 through 6-15 should not exceed 2 Ω impedance. The material in these zones should be galvanically compatible with electroplated tin and should not contain holes, silkscreening, or protrusions.

OBSERVATION 6.1.4-2:
The module zones called out with Note 6.1.4-1 in figures 6-8 through 6-15 come in contact with shielding ground springs in some mainframes. These shielding ground springs improve the EMC performance of the system and are not intended as safety grounds. A mainframe is not required to have shielding ground springs that insure a ground path through these zones.

RULE 6.1.4-3:
All module zones called out with Note 6.1.4-3 in figures 6-9, 6-11, 6-13, and 6-15 **MUST NOT** have any holes larger than 10 mm in diameter on top of the module or 6 mm in diameter on the sides of the module. These zones **MUST NOT** contain silkscreening, labels, or protrusions.

OBSERVATION 6.1.4-4:
The module zones called out with Note 6.1.4-3 in figures 6-9, 6-11, 6-13, and 6-15 come in contact with shielding ground springs in some mainframes. To guarantee that repeated module removal and replacement will not damage any mainframe shielding springs, these zones should be free of any features.

OBSERVATION 6.1.4-5:
The most effective EMC grounding path between a module and a mainframe is typically through the mainframe bottom rear ground spring (item 26), figures 6-40 and 6-51.

6.1.5 Module Mass

RULE 6.1.5-1:
The module mass **MUST** be included in module specification and data sheets.

SUGGESTION 6.1.5-2:
When practical, module designs should place the center of mass toward the front of the module (z axis) and toward the bottom of the module (y axis), figure 6-3.

OBSERVATION 6.1.5-3:
The structural support of the module in the mainframe is provided by two mechanical interfaces. These are the module front "V" feature (Module Datum B), figure 6-4, and the module primary rear bushing (item 10, Module Datum D), figure 6-8, on the rear of the module. In a well designed mainframe, the weakest link is expected to be the mainframe guide pin (item 24, Mainframe Datum D), figure 6-31. By placing the module center of mass toward the front of the module, stress in the mainframe guide pin(s) will be reduced.

OBSERVATION 6.1.5-4:
The maximum single module mass that can be supported in an MMS system is a function of the module mass distribution, environmental requirements, and the individual module and mainframe mechanical designs.

RECOMMENDATION 6.1.5-5:
Modules which have a mass greater than 5 kilograms should incorporate a module secondary rear bushing (Module Datum J), figures 6-6 and 6-14.

OBSERVATION 6.1.5-6:
The module secondary rear bushing (Module Datum J), figures 6-6 and 6-14, helps to stabilize the module during shock and vibration. It also helps to lower stress by distributing force to multiple mainframe guide pins (item 24, Mainframe Datum D), figure 6-31.

6.1.6 Module Microphonic Vibration

RECOMMENDATION 6.1.6-1:
If an MMS module produces microphonic vibration, then the operating mode under which it is produced should be specified by the MMS module manufacturer.

RECOMMENDATION 6.1.6-2:
If an MMS module is sensitive to microphonic vibration, then this should be specified by the MMS module manufacturer.

SUGGESTION 6.1.6-3:
Modules should incorporate damping and isolation for vibration sensitive components and also for any devices (e.g. disk drives) which generate vibration. A large margin between the vibration sensitivity of a module and the .010 g mainframe microphonic vibration limit (rule 6.2.4-1) is desirable.

6.1.7 Module Environmental

OBSERVATION 6.1.7-1:
It is the responsibility of the MMS system integrator to select modules and mainframes that will meet the environmental requirements of the specific application.

6.1.8 Module Industrial Design

SUGGESTION 6.1.8-1:
MMS modules should be designed according to the specifications given in figures 6-56 through 6-66 and 6-68 through 6-77 for module front and module rear component placement.

OBSERVATION 6.1.8-2:
Designing to the specifications given in figures 6-56 through 6-66 and 6-68 through 6-77 insures consistent MMS system appearance and human interface, and standard intermodular cabling.

RULE 6.1.8-3:
If a front panel or rear panel is used as the module front or module rear as shown in figures 6-56 and 6-68 through 6-69, then the panels **MUST** be contained within the module envelope specifications given in figures 6-8 through 6-15.

SUGGESTION 6.1.8-4:
If a front panel is used for the module front, then figure 6-56 shows the panel size and positional tolerance that should be used to insure consistent MMS module appearance.

OBSERVATION 6.1.8-5:
Figures 6-56 and 6-68 depict specifications for 1, 2, 3, and 4 slot modules. Width dimensions for modules greater than 4 slots can be calculated using the following formulas:

$$\text{Front Panel Width} = (47.6 + (N\text{-}1) \times 48.39) \pm 0.08$$

$$\text{Rear Panel Width} = (41.5 + (N\text{-}1) \times 48.39) \pm 0.02$$

where,

N = number of slots
dimensions are in mm

RULE 6.1.8-6:
Module front indicator color **MUST** be selected based on the indicator application as shown in figure 6-67.

RULE 6.1.8-7:
MMS modules **MUST** use the module system address graphics shown in figure 6-78.

6.2 Mainframe Specifications

6.2.1 Mainframe Envelope/ Interface

RULE 6.2.1-1:
MMS mainframes **MUST** be designed according to the specifications given in figures 6-29 through figure 6-41.

OBSERVATION 6.2.1-2:
Figures 6-27 and 6-28 give an overview of the principal mainframe datums and their functions. These datums are used throughout figures 6-29 through 6-41.

RULE 6.2.1-3:
Every MMS mainframe slot **MUST** have one mainframe latch assembly (items 1,12,20-23), figure 6-47.

RULE 6.2.1-4:
Every MMS mainframe slot **MUST** have one mainframe guide pin (item 24, Mainframe Datum D), figure 6-31.

RULE 6.2.1-5:
Every MMS mainframe slot **MUST** have a mainframe channel as shown in figure 6-35. This channel **MUST** be on the same centerline as the mainframe guide pin (item 24, Mainframe Datum D), figure 6-31.

RULE 6.2.1-6:
MMS mainframes **MUST** be designed to allow complete access to the module front and rear access/extension areas, figure 6-8, when a module is fully engaged into a mainframe. Figure 6-41 shows the location of the module rear user access/extension area in relation to a mainframe guide pin, (item 24, Mainframe Datum D), figure 6-31, when a module is fully engaged into a mainframe.

PERMISSION 6.2.1-7:
Any part of the module front outside of the module front access/extension area, figure 6-8, **MAY** be covered (e.g. behind a door) or be otherwise inaccessible after being fully engaged into a mainframe.

OBSERVATION 6.2.1-8:
The mainframe channel shown in figure 6-35 acts as the guiding feature for the module rear alignment feature, figure 6-9. Together, these two features insure proper mating of the mainframe guide pin (item 24, Mainframe Datum D), figure 6-31, and the module primary rear bushing (item 10, Module Datum D), figure 6-8.

RECOMMENDATION 6.2.1-9:
Every MMS mainframe slot should use a vibration stop (item 28), figure 6-52, as shown in figure 6-37.

OBSERVATION 6.2.1-10:
In a high vibration environment, the vibration stop (item 28), figure 6-52, limits movement of the top of the module in the x-axis.

OBSERVATION 6.2.1-11:
A nominal 1.0 mm offset exists between Module Datum A (module front rear face) and Mainframe Datum A (mainframe front face) when the module is fully engaged into the mainframe as shown in figures 6-3 and 6-28.

6.2.2 Mainframe MSIB Connector

6.2.2.1 Internal

RULE 6.2.2.1-1:
The mainframe MSIB connector (item 29) **MUST** be designed according to the specifications given in figure 6-53. All dimensions apply after plating.

RULE 6.2.2.1-2:
Every MMS mainframe slot **MUST** have one mainframe MSIB connector (item 29), figure 6-53.

RULE 6.2.2.1-3:
The indexing boss feature (mainframe connector item 3) of the mainframe MSIB connector (item 29), figure 6-53, **MUST** be oriented in the mainframe as shown in figure 6-36.

OBSERVATION 6.2.2.1-4:
The indexing boss feature (mainframe connector item 3) of the mainframe MSIB connector (item 29), figure 6-53, polarizes the mainframe/module MSIB connector pair.

OBSERVATION 6.2.2.1-5:
The connector pin assignments for the mainframe MSIB connector (item 29), figure 6-53, are shown in appendix A.1.

RULE 6.2.2.1-6:
The mechanical durability of the mainframe MSIB connector (item 29), figure 6-53, **MUST** be a minimum of 500 insertion/extraction cycles when measured per EIA STD RS-364-09.

RULE 6.2.2.1-7:
The insulation resistance of the mainframe MSIB connector (item 29), figure 6-53, **MUST** be a minimum of 5000 MΩ at 500 VDC when measured per EIA STD RS-364-21A.

RULE 6.2.2.1-8:
The dielectric of the mainframe MSIB connector (item 29), figure 6-53, **MUST** withstand 1500 VAC for 60 seconds when tested per EIA STD RS-364-20A Method A at sea level.

RULE 6.2.2.1-9:
The current rating of the mainframe MSIB connector (item 29), figure 6-53, **MUST** be 3.0 amps per contact.

RULE 6.2.2.1-10:
The current resistance of the mainframe MSIB connector (item 29), figure 6-53, **MUST** be 8.3 mΩ maximum per mated contact at rated current and temperature range.

RULE 6.2.2.1-11:
The mainframe MSIB connector (item 29), figure 6-53, **MUST** be able to sustain continuous operation within a temperature range of -55° C to +95° C without a reduction in mechanical or electrical performance.

SUGGESTION 6.2.2.1-12:
Identification of pin contact positions (i.e. 1,11,22,29,40 and 50 as shown in figure 6-53) on the mainframe MSIB connector can be helpful.

RULE 6.2.2.1-13:
The indexing boss feature (mainframe connector item 3) of the mainframe MSIB connector (item 29), figure 6-53, **MUST** be aligned as shown in figure 6-53 and held in position to within ± 2° with Mainframe Connector Datum Y as reference.

RECOMMENDATION 6.2.2.1-14:
The material specifications for mainframe connector items 1 thru 5 should be as follows:

1. **Plug Body:** 30% glass reinforced PET, PETRA 130 FR or RYTON R4 (P.P.S. per MIL-P-46174, Class 40).
2. **Guide Pin:** CRES type 303 per ASTM-A581; passivate per QQ-P-35.
3. **Indexing Boss:** Aluminum alloy 7075-T6 per QQ-A-225/9; electroless nickel plate per MIL-C-26074 Class I (0.0013-0.0025mm thk) over copper per MIL-C-15540.
4. **Securing Cap:** Aluminum alloy 6061-T6 per QQ-A-225/9; chromate conversion per MIL-C-5541.
5. **Pin Contact:** Beryllium copper per ASTM B196, alloy UNS No. C17300, temper TH04; gold plate 0.00076mm min. over 0.0013mm min. nickel plate; test per EIA STD RS-364-53.

RULE 6.2.2.1-15:
The mainframe MSIB connector (item 29), figure 6-53, **MUST** be able to withstand a torque applied to its indexing boss feature (mainframe connector item 3) of 0.7 N-m. The mainframe MSIB connector **MUST NOT** exhibit any reduction in its electrical or mechanical specifications after this torque has been applied.

6.2.2.2 External

RULE 6.2.2.2-1:
If external MSIB connectors are provided, then they **MUST** conform to ISO standard 2110 or MIL-C-24308 and be of the following type..

- **MSIB out:** 2 row, 37 contact, low profile male D-subminiature.
- **MSIB in:** 2 row, 37 contact, low profile female D-subminiature.

OBSERVATION 6.2.2.2-2:
The connector pin assignments for the external MSIB connectors are shown in appendix A.2.

6.2.3 Mainframe EMC Grounding

PERMISSION 6.2.3-1:
MMS mainframes **MAY** use mainframe grounding springs to improve the EMC performance of the system.

RULE 6.2.3-2:
If mainframe grounding springs are used, then they **MUST** be positioned in the mainframe such that they will be in contact with the module zones called out with Note 6.1.4-1 in figures 6-8 thru 6-15, as shown in figure 6-40, when the module is fully installed into the mainframe.

RULE 6.2.3-3:
If mainframe grounding springs are used, then they **MUST** be designed to be able to slide over holes 10mm in diameter on the top of modules and 6mm in diameter on the sides of modules in all module zones called out with Note 6.1.4-3 in figures 6-9, 6-11, 6-13, and 6-15.

RULE 6.2.3-4:
If mainframe grounding springs are used, then they **MUST** be designed to withstand a minimum of 500 module installation/removal cycles.

OBSERVATION 6.2.3-5:
MMS systems (both modules and mainframes) are designed for a minimum of 500 module installation/removal cycles.

SUGGESTION 6.2.3-6:
The top front ground spring (item 25), figure 6-49, bottom rear ground spring (item 26), figure 6-51, and top rear ground spring (item 27), figure 6-50, can be used as the mainframe grounding springs as shown in figure 6-40. These springs have been designed with a 2 Ω maximum impedance.

SUGGESTION 6.2.3-7:
If intermodular ground springs or additional mainframe grounding springs are required to achieve adequate EMC performance, then those springs should be positioned in the mainframe or on the modules such that they will be in contact with the module zones called out with Note 6.1.4-3 in figures 6-9, 6-11, 6-13, and 6-15.

OBSERVATION 6.2.3-8:
The most effective EMC grounding path between a module and a mainframe is typically through the mainframe bottom rear ground spring (item 26), figures 6-40 and 6-51.

6.2.4 Mainframe Microphonic Vibration

RULE 6.2.4-1:
Microphonic vibration produced by an unloaded mainframe **MUST NOT** exceed .010 g's at any frequency or operating voltage. It **MUST** be measured in three axes on both the mainframe front and mainframe rear, with the mainframe front face (Mainframe Datum A), figure 6-28, as a reference. See appendix B.4 for *Mainframe Microphonic Vibration Test Procedure*.

OBSERVATION 6.2.4-2:
Compliance with rule 6.2.4-1 does not guarantee that design problems with microphonic vibrations will not occur.

SUGGESTION 6.2.4-3:
Mainframes should incorporate damping and isolation for fans and other vibration generating devices. A large margin between the vibrational output of a mainframe and the 0.010 g limit is desirable.

6.2.5 Mainframe Environmental

OBSERVATION 6.2.5-1:
It is the responsibility of the MMS system integrator to select modules and mainframes that will meet the environmental requirements of the specific application.

6.3 Figures
The figures referred to in sections 6.1 and 6.2 are on the following pages.

GENERAL NOTES FOR MODULE AND MAINFRAME CONSTRUCTION

NOTES: UNLESS OTHERWISE SPECIFIED

1. INTERPRET ALL FIGURES ACCORDING TO ANSI Y14.5M-1982.
2. ALL DIMENSIONS SHOWN ARE IN MILLIMETERS.
3. KEY TO FIGURE SYMBOLS: (X) REFERS TO ITEM NUMBER FOR ASSEMBLY PURPOSES. SEE MODULE OR MAINFRAME MATERIAL LISTS (FIG 6-16 & -42).
   [X] REFERS TO NOTE CALL OUT, SEE CORRESPONDING NUMBER IN GENERAL NOTES OR TEXT.
   ⟨X⟩ REFERS TO A REVISION OF DATA FROM PREVIOUS PUBLICATIONS.
4. DETAILS AND DIMENSIONS SHOWN IN FIGURES 6-4 THRU 6-7 ARE COMMON TO ALL MODULES. FOR DIMENSIONS NOT SHOWN ON FIGURES 6-8 THRU 6-15 REFER TO THE NEXT NUMERICALLY DECENDING FIGURE.

[5] RECOMMENDATION:
LIGHTLY COAT RUBBER 'O'RING (ITEM 1) WITH STEM GREASE (OR EQUIV. ITEM 12)BEFORE INSTALLING MODULE LATCH INTO THE MODULE FRONT (FIG 6-4).

[6] RECOMMENDATION:
IF FEATURE IS CAST INTO PART, MAXIMUM +2° DRAFT IS ALLOWABLE. DIMENSION TO READ +DR (FIG 6-4 & -5).

[7] RULE:
PINS ITEM 8 AND BUSHINGS ITEM 10 TO BE PRESS FIT INTO THE REAR FRAME AND INSTALLED FLUSH TO SUB FLUSH TO OUTER SURFACE DATUM E (FIG 6-5,-7 & -14).

[8] OBSERVATION:
MAXIMUM POSITION OF MAINFRAME GUIDE PIN INTO THE INTERIOR OF MODULE (FIG 6-7 &-10).

[9] RULE:
THESE FEATURES ARE CLEARANCES FOR MAINFRAME CONNECTORS, GUIDE PIN AND LATCHES ON THE 2,3 & 4 SLOT MODULES WHEN THE MODULE IS FULLY ENGAGED INTO THE MAINFRAME (FIG 6-10,-12 & -14).

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- THIRD ANGLE PROJECTION
- TOLERANCES

~~XX ± 0.5mm or ±~~
~~XX.X ± 0.2mm or~~ ±0.4
XX.XX ± 0.1mm or ±
~~ALL ± ------ mm~~

- ADHERENCE TO MMS SPECIFICATION APPENDIX C REQUIRED
- DO NOT SCALE THIS DRAWING

META-C

TABLE 6-1. General Notes for Module and Mainframe Construction

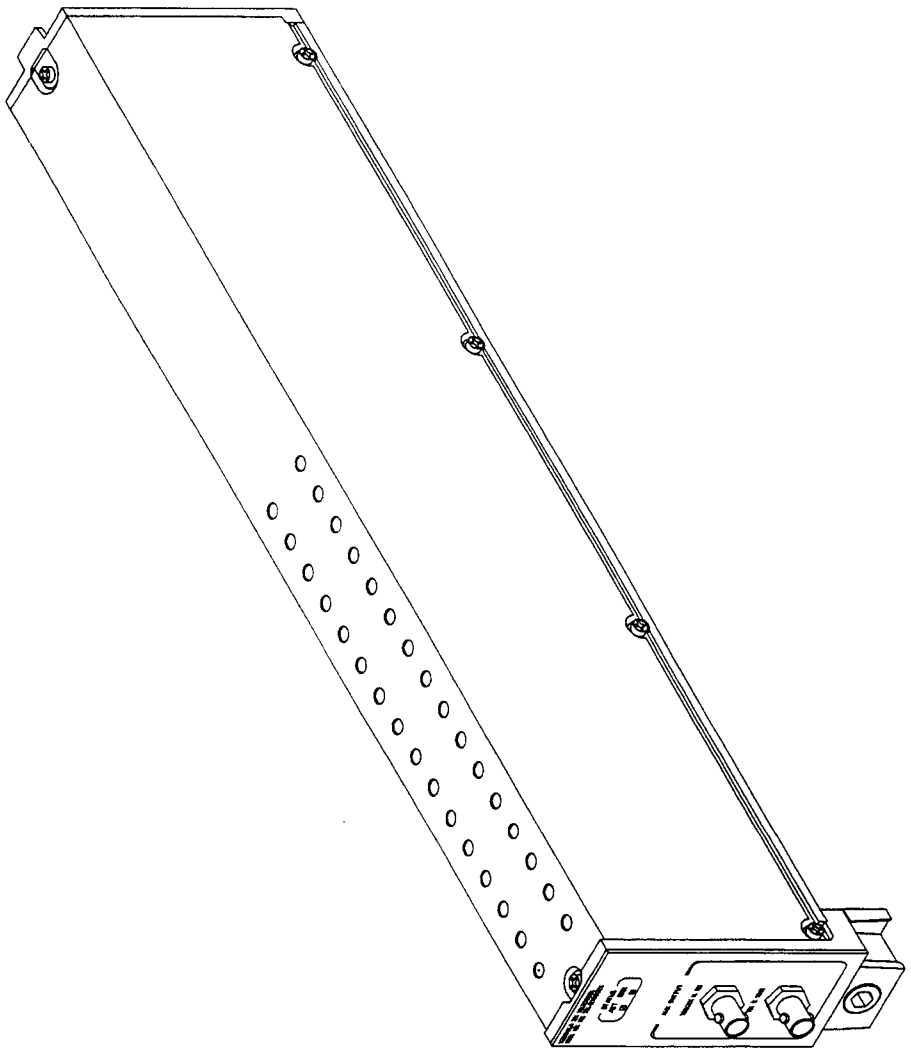


FIGURE 6-1. ISOMETRIC VIEW OF 1 SLOT MODULE

MODULE DATUM ORIGINS AND EXPLANATIONS			
	DATUM	ORIGIN	FUNCTION
1.	-A-	MODULE FRONT REAR FACE (FIGURE 6-4)	PRIMARY DATUM FOR FRONT FRAME DETAILS.
2.	-B-	MODULE FRONT "V"FEATURE (FIGURE 6-4)	SECONDARY DATUM FOR FRONT FRAME DETAILS.
3.	-C-	MODULE FRONT LOCATION TAB (FIGURE 6-4)	TERTIARY DATUM FOR FRONT FRAME DETAILS.
4.	-D-	MODULE PRIMARY REAR BUSHING (FIGURE 6-5)	SECONDARY DATUM FOR REAR FRAME DETAILS.
5.	-E-	MODULE REAR FACE (FIGURE 6-5)	PRIMARY DATUM FOR REAR FRAME DETAILS.
6.	-F-	MODULE FRONT LATCH THRU HOLE (FIGURE 6-4)	POSITIONAL CONTROL FOR LATCH COUNTERBORE.
7.	-G-	MODULE REAR SPRING PIN HOLES (FIGURE 6-5)	POSITIONAL CONTROL FOR SPRING PIN COUNTERBORE HOLES.
8.	-H-	MODULE REAR LOCATION TAB (FIGURE 6-9)	TERTIARY DATUM FOR REAR FRAME DETAILS.
9.	-J-	MODULE SECONDARY REAR BUSHING (FIGURE 6-6)	POSITIONAL CONTROL FOR ADDITIONAL CONNECTORS.

FIGURE 6-2. EXPLANATION OF MODULE DATUMS

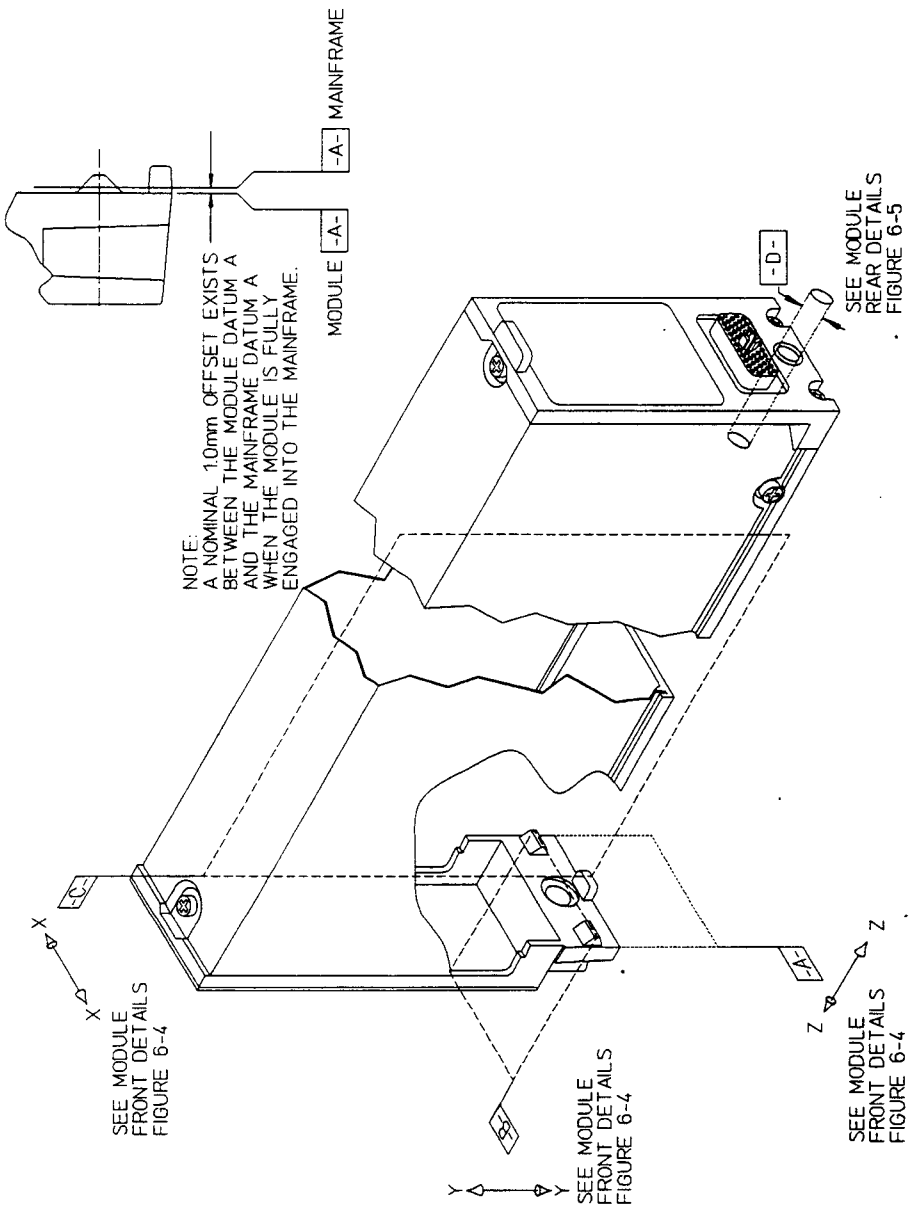
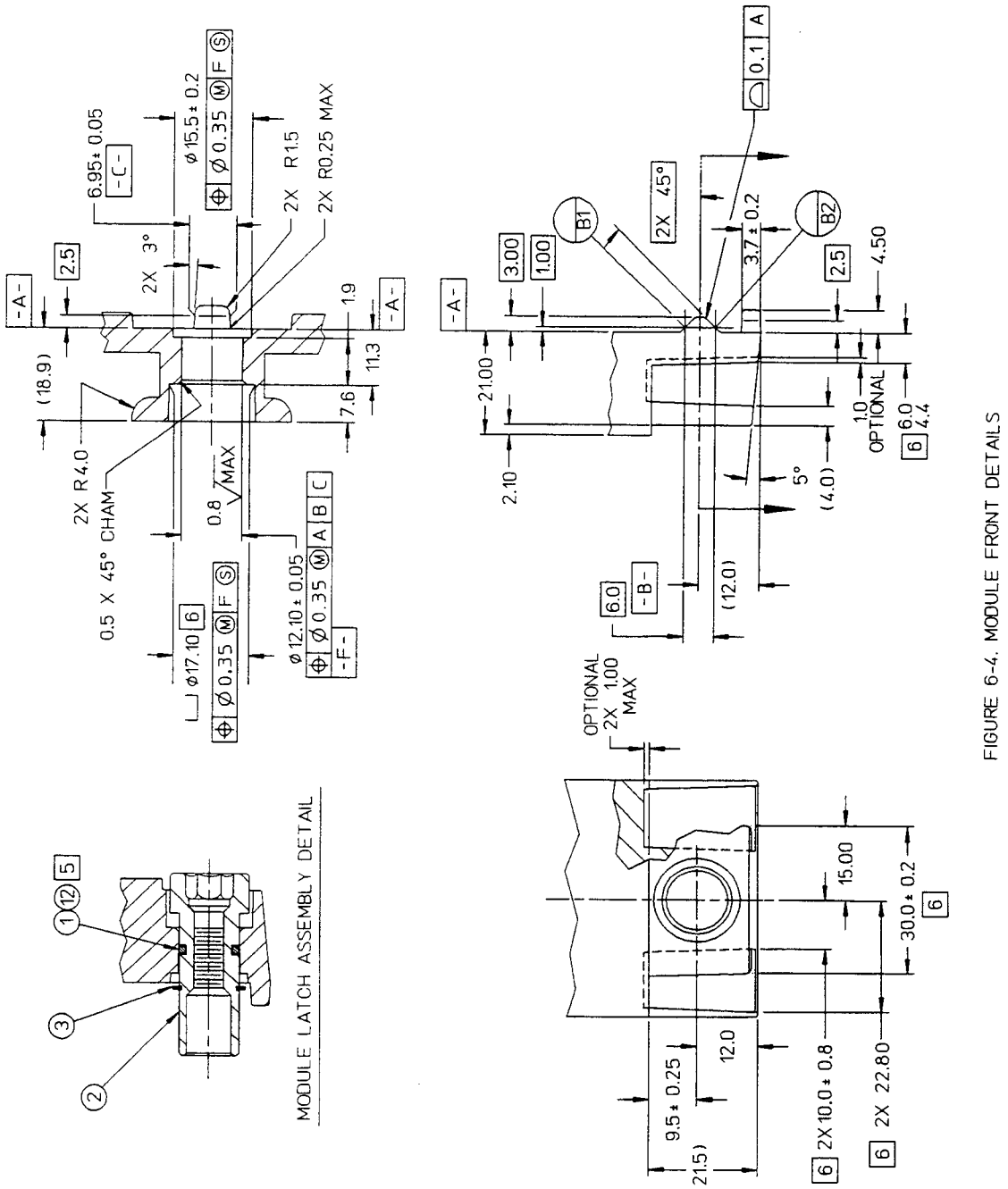


FIGURE 6-3. DIAGRAM OF PRINCIPLE MODULE DATUMS


MODULE LATCH ASSEMBLY DETAIL
FIGURE 6-4. MODULE FRONT DETAILS

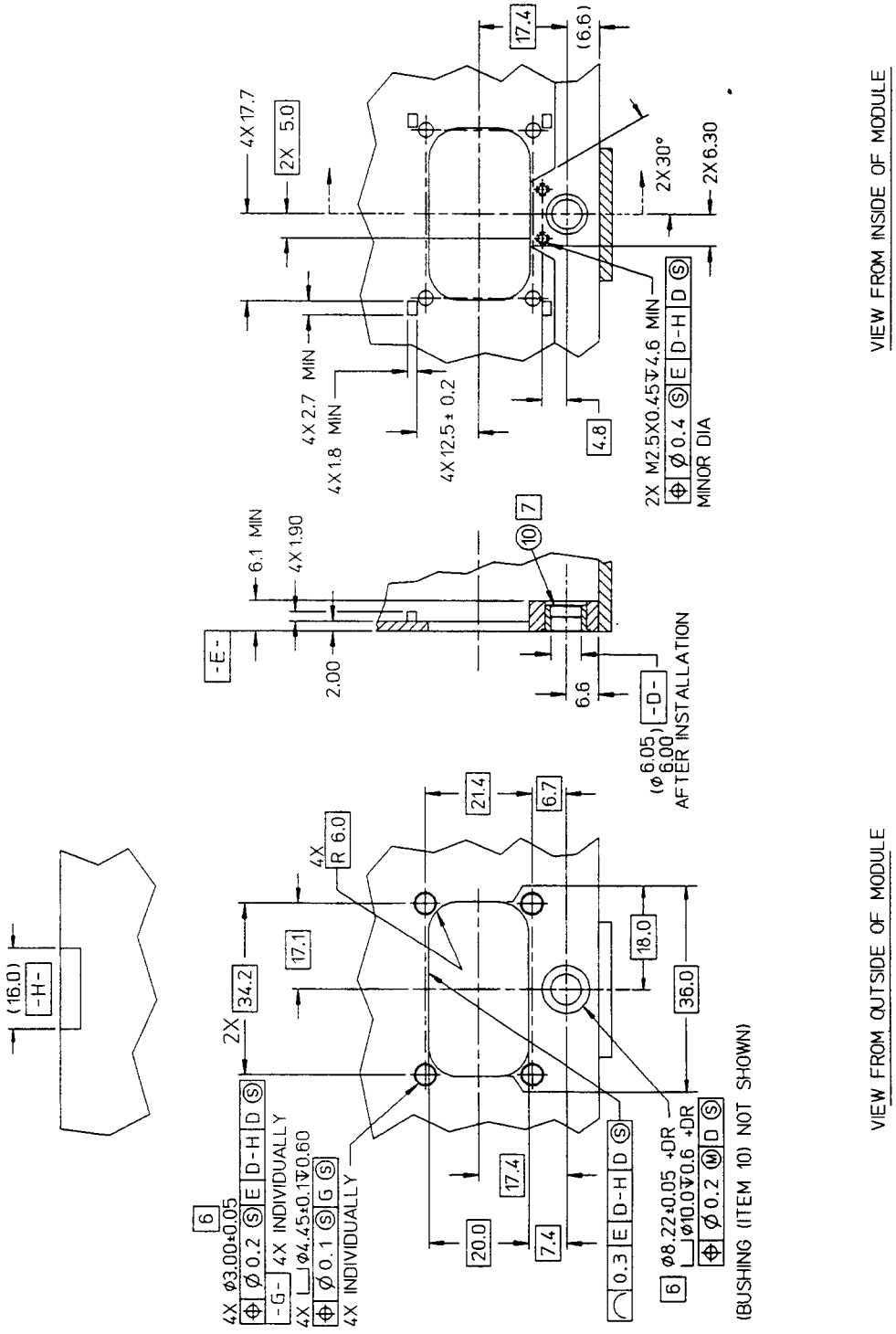


FIGURE 6-5. MODULE REAR DETAILS

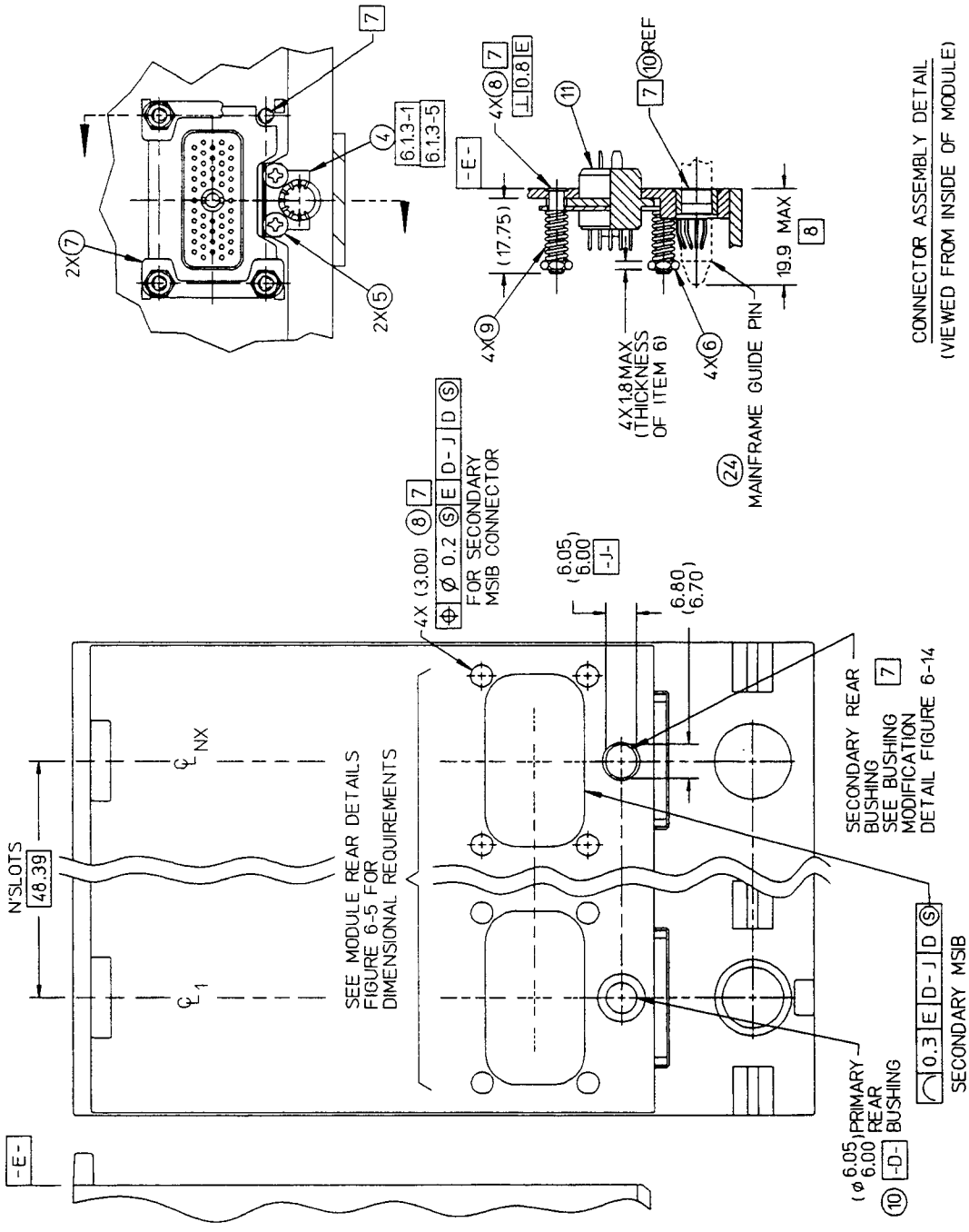


FIGURE 6-6. MODULE REAR DETAILS FOR MULTIPLE CONNECTORS & BUSHINGS

FIGURE 6-7. MODULE REAR, CONNECTOR ASSEMBLY

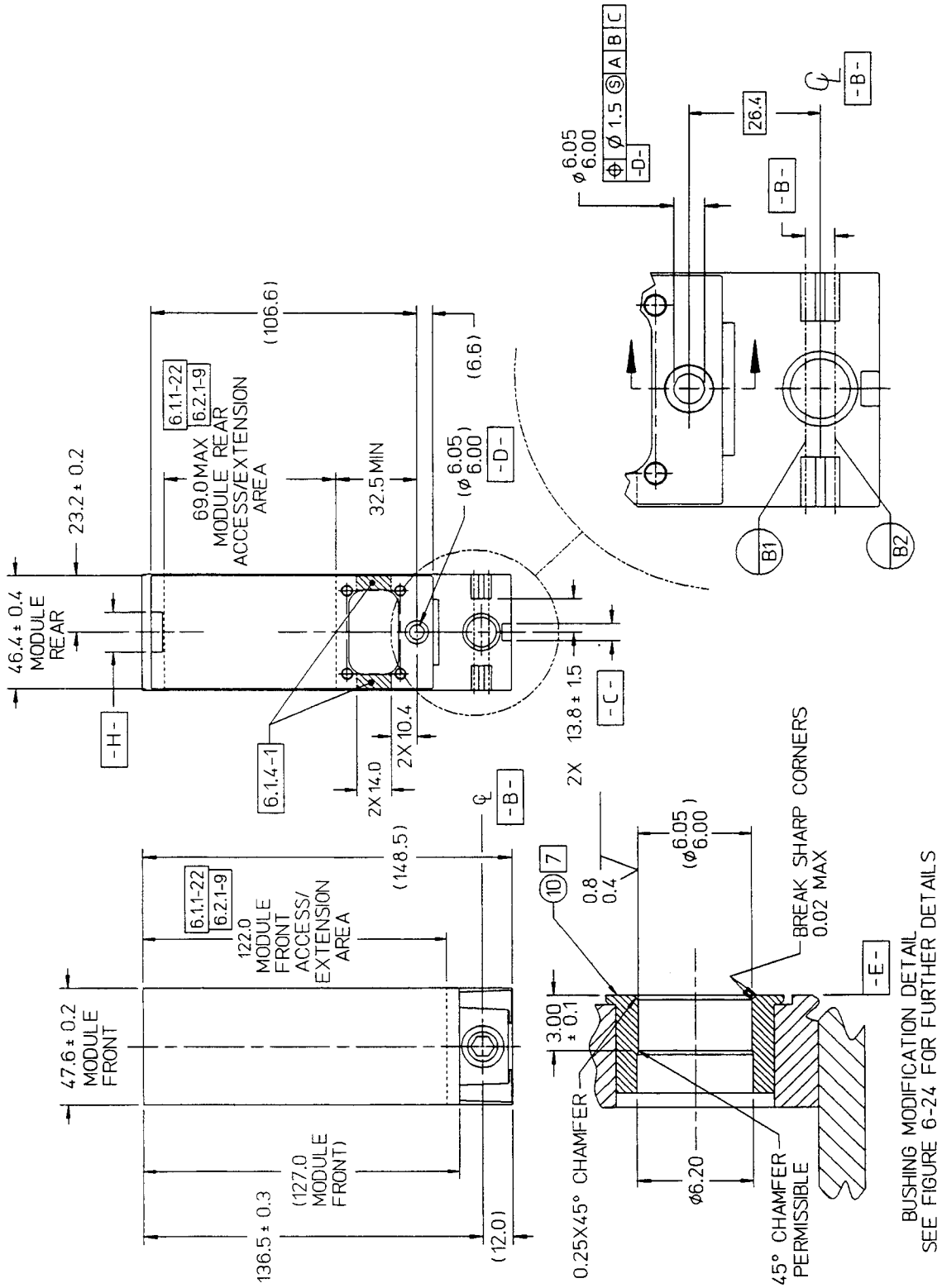


FIGURE 6-8. 1 SLOT MODULE FRONT & REAR DETAILS

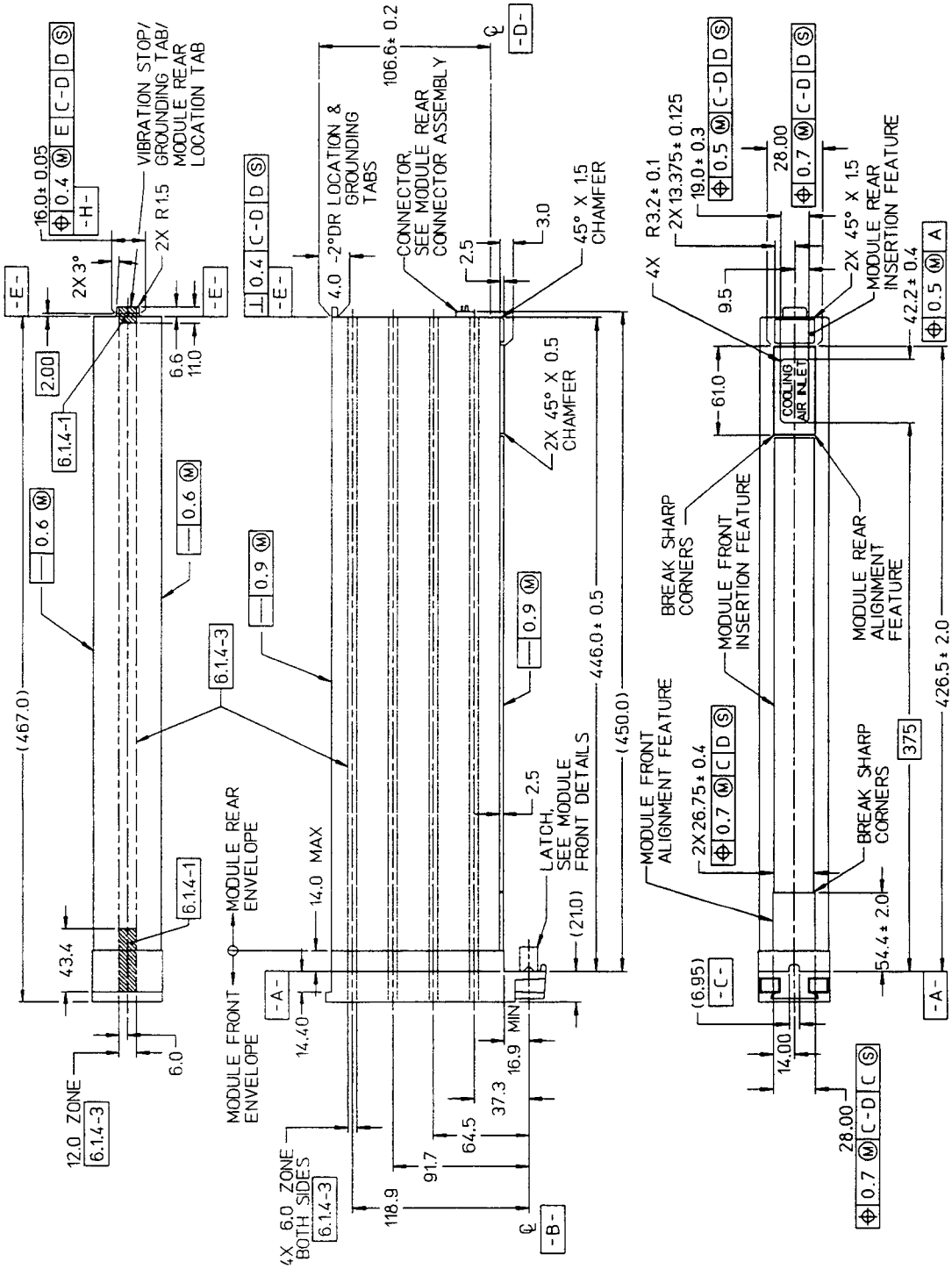


FIGURE 6-9. 1 SLOT MODULE TOP, SIDE & BOTTOM DETAILS

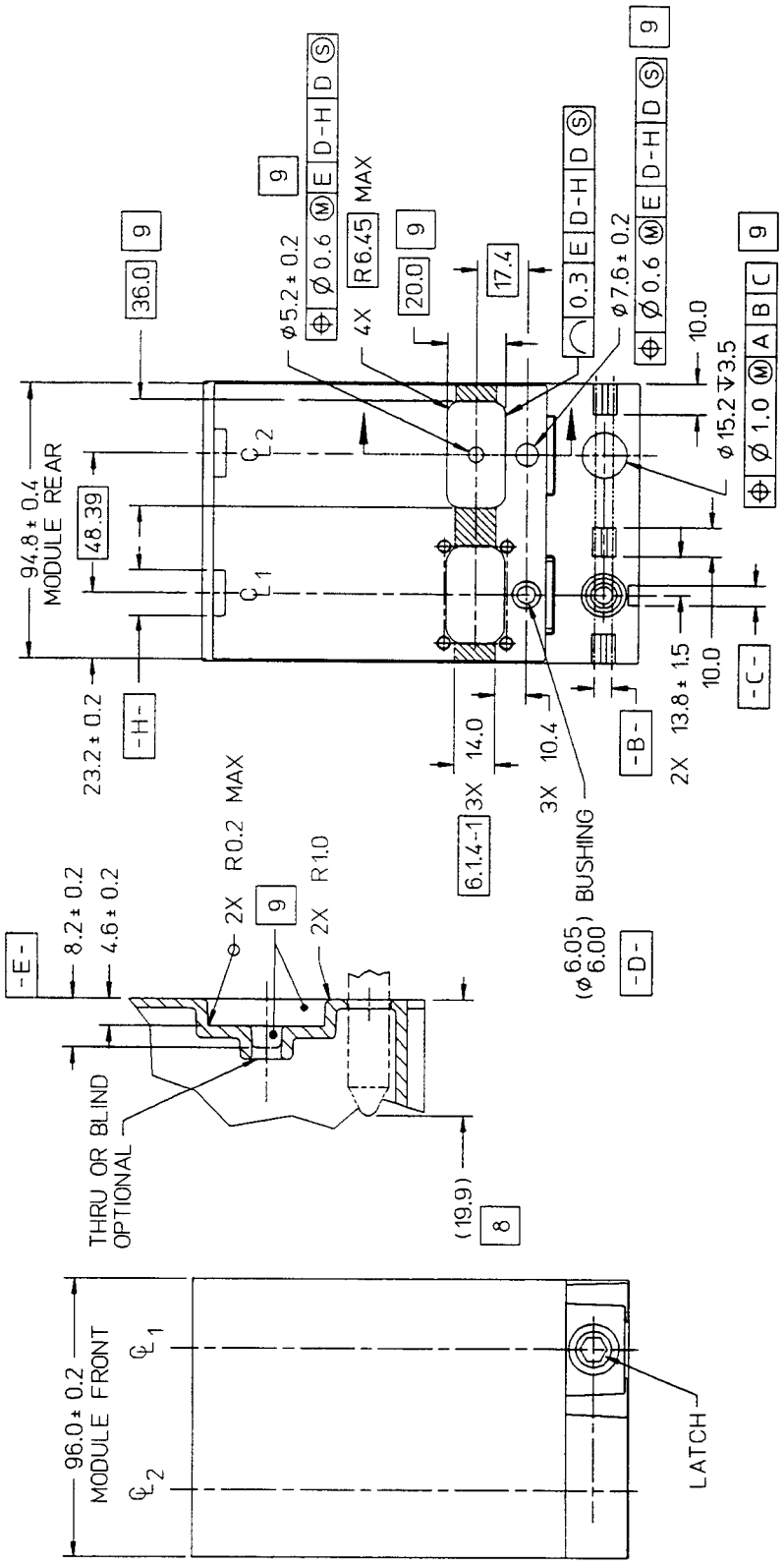


FIGURE 6-10. 2 SLOT MODULE FRONT & REAR DETAILS

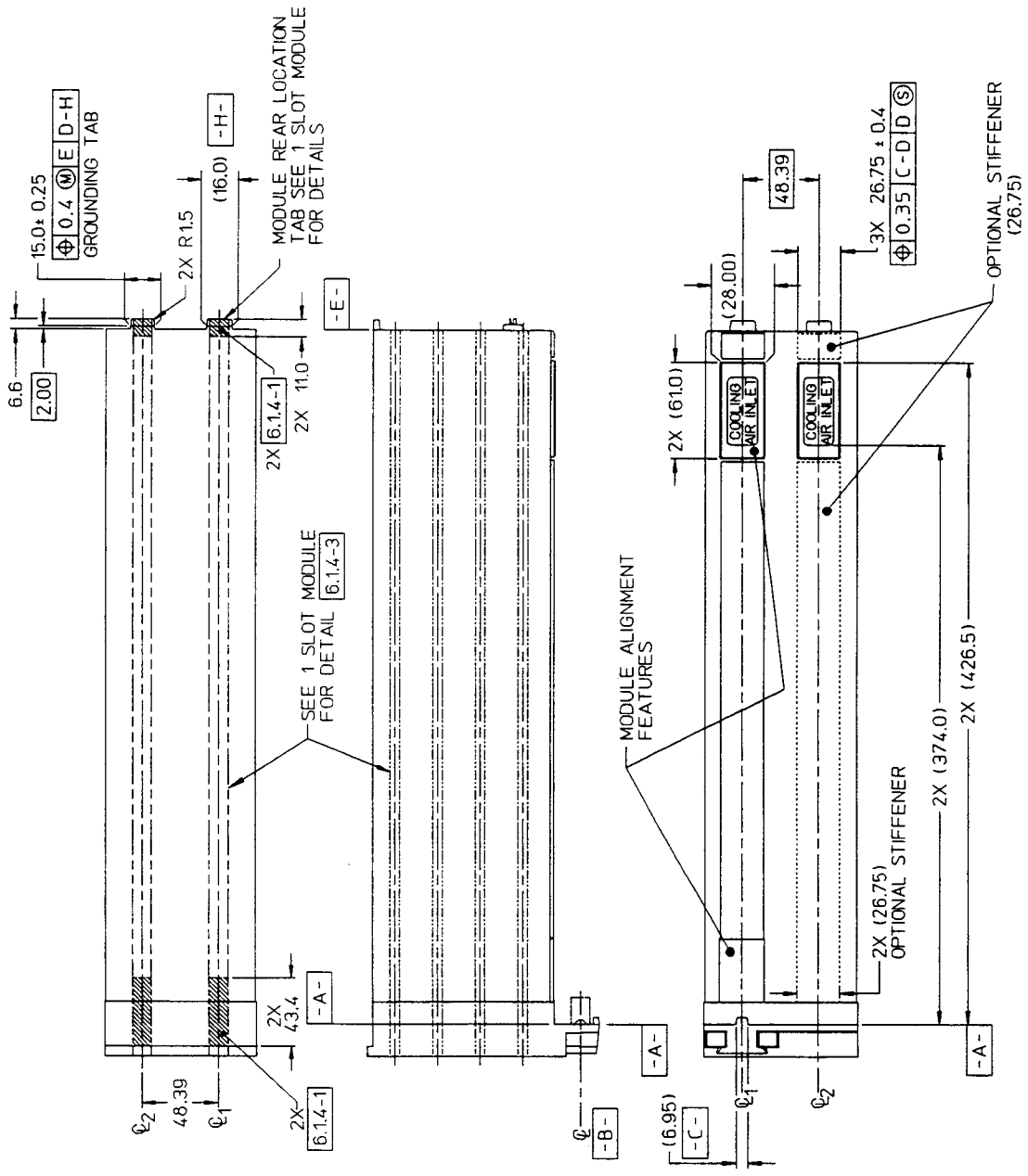


FIGURE 6-11. 2 SLOT MODULE TOP, SIDE & BOTTOM DETAILS

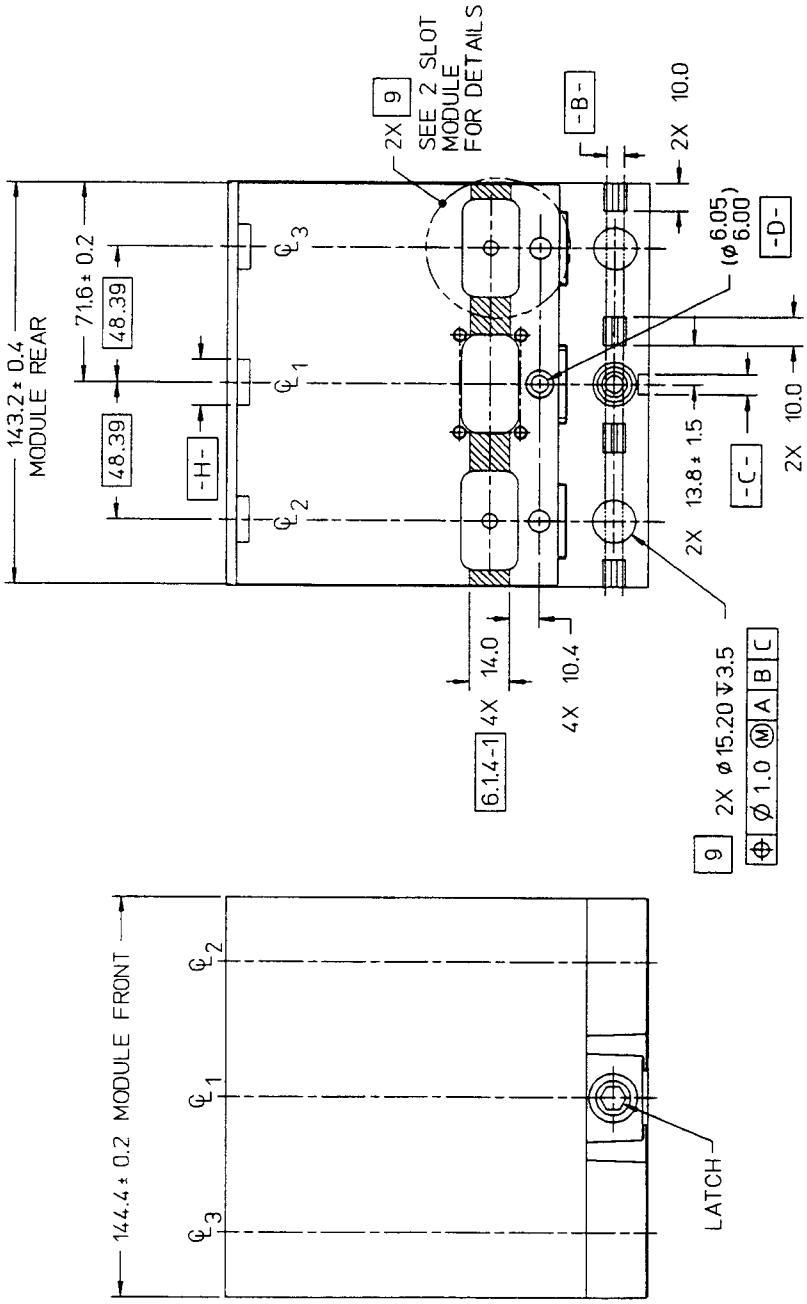


FIGURE 6-12. 3 SLOT MODULE FRONT & REAR DETAILS

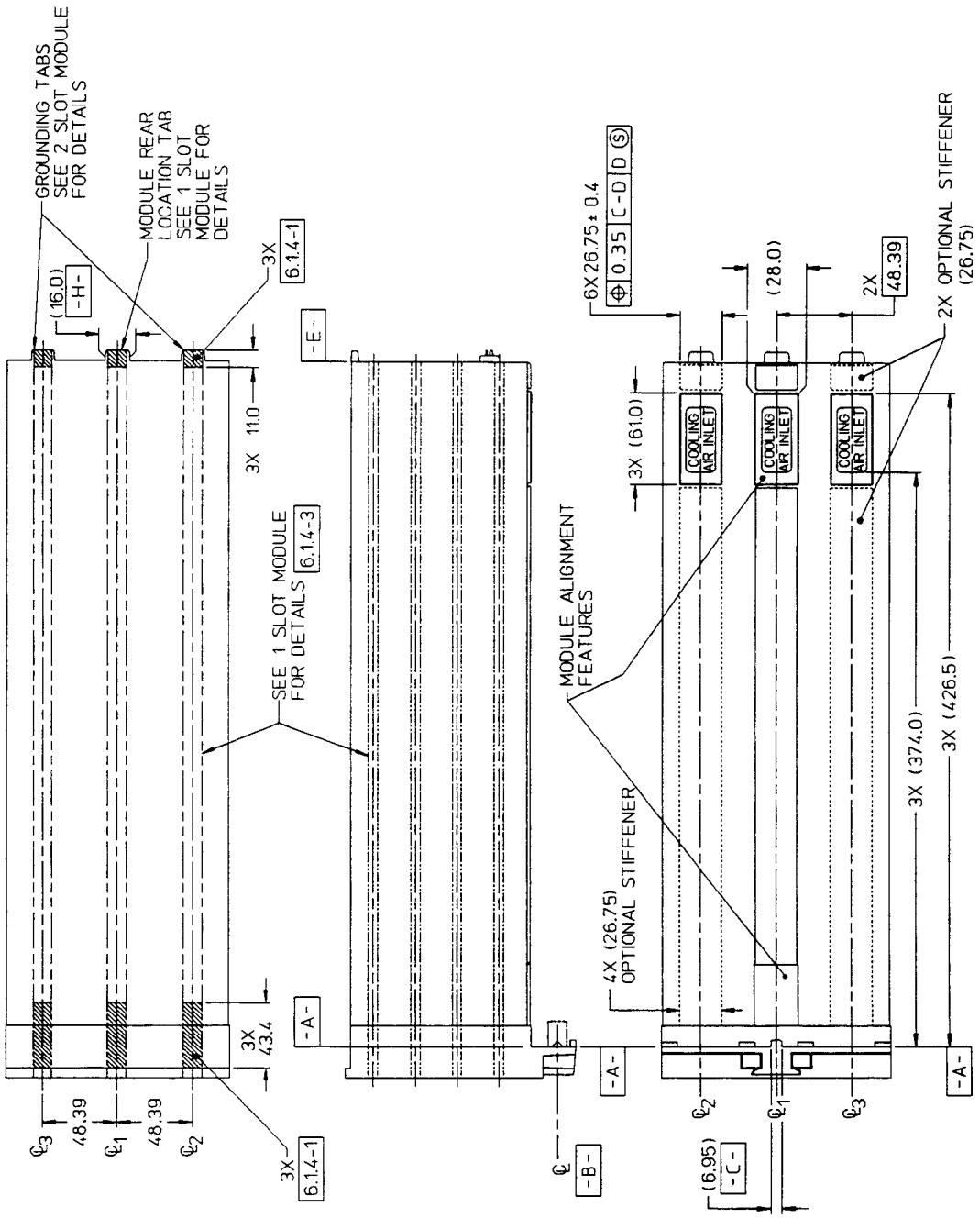


FIGURE 6-13. 3 SLOT WIDE MODULE TOP, SIDE & BOTTOM DETAILS

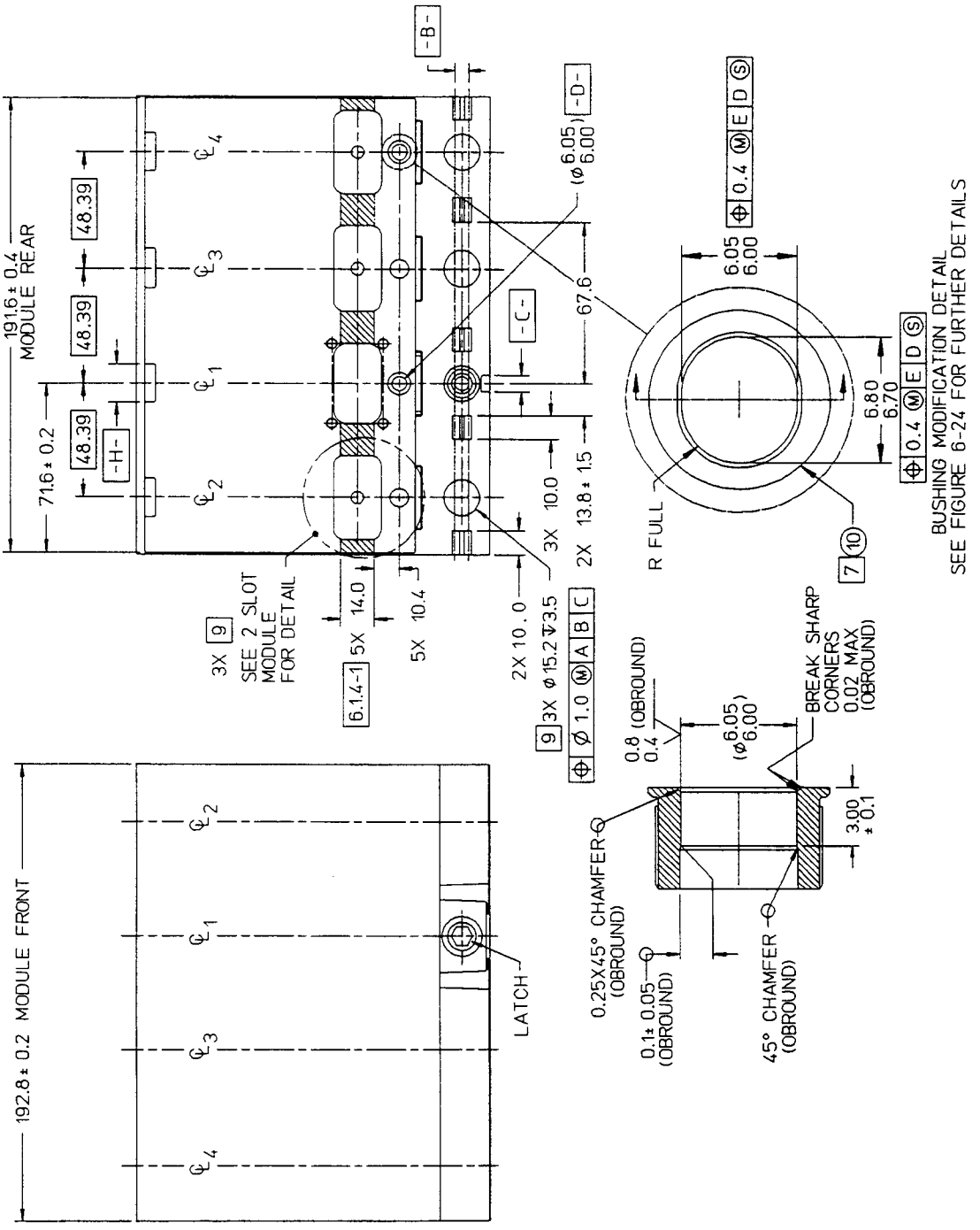


FIGURE 6-14. 4 SLOT MODULE FRONT & REAR DETAILS

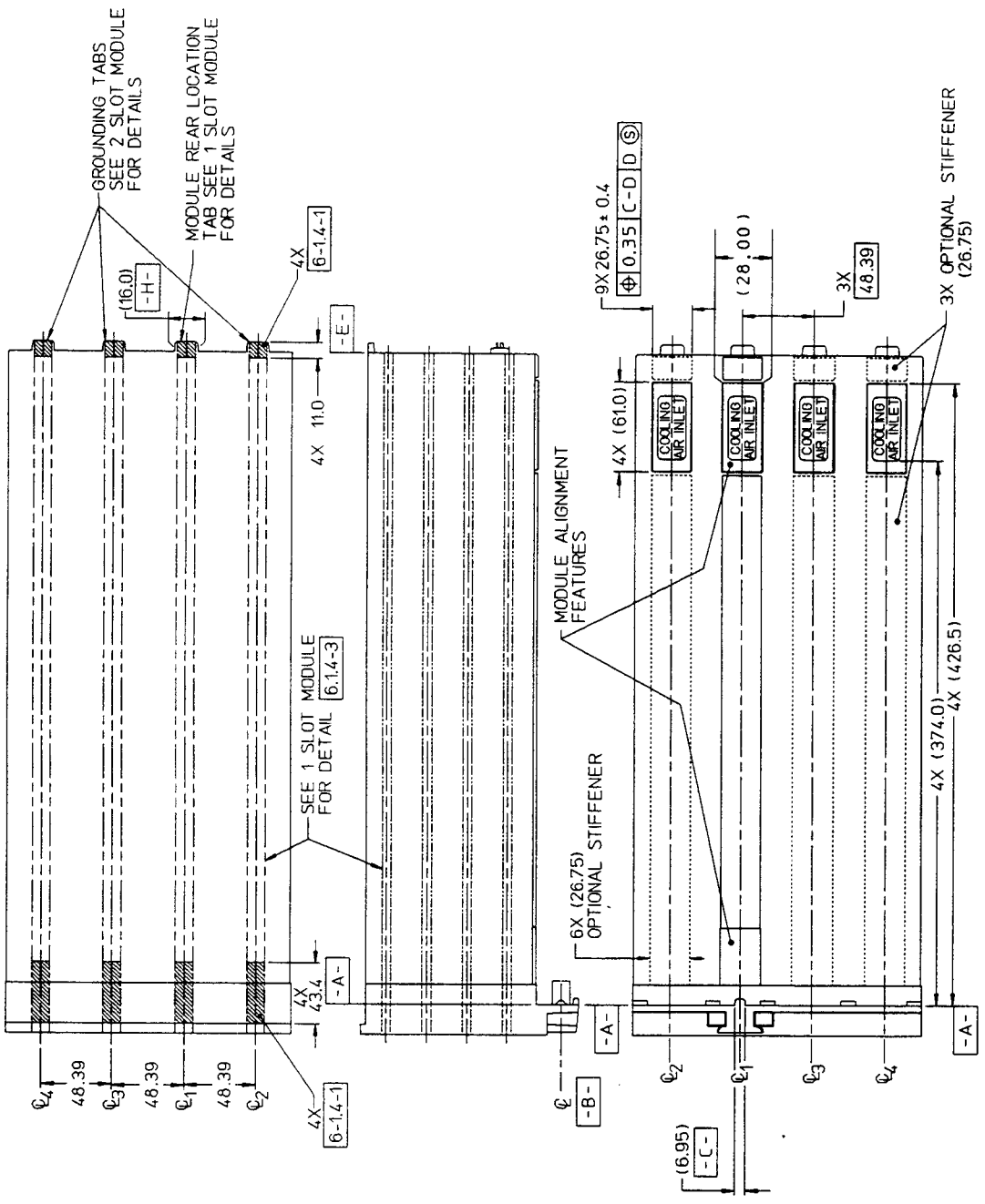
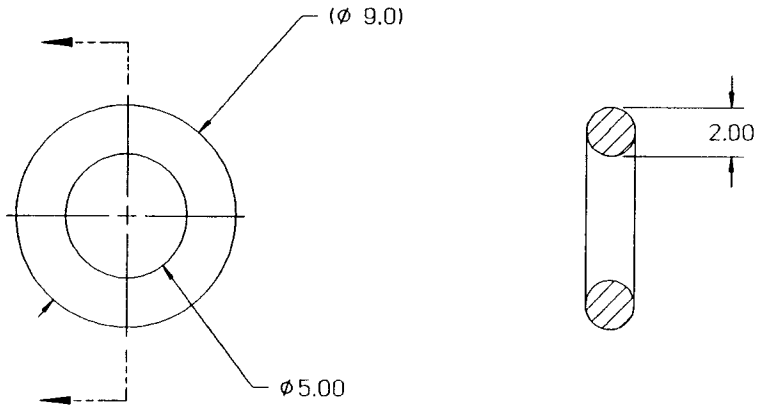


FIGURE 6-15. 4 SLOT WIDE MODULE TOP, SIDE & BOTTOM DETAILS

MATERIAL LIST FOR MODULE ASSEMBLY

	ITEM	QTY	MAT'L DESCRIPTION	FIG.#
RULE	1	1	O-RING	6-17
RULE	2	1	LATCH, MODULE	6-19
RULE	3	1	RETAINING RING	6-18
OBSERVATION	4	1	SPRING, GROUNDING	6-20
SUGGESTION	5	2	SCREW, PN HD, M2.5 X 4L CRES	NONE
RULE	6	4	NUT, M3 1.8mm THICK MAX	NONE
RULE	7	2	BAR, CONNECTOR	6-21
RULE	8	4	PIN, SPRING	6-23
RULE	9	4	SPRING, COMPRESSION	6-22
RULE	10	A/R	BUSHING	6-24
RULE	11	1	CONNECTOR, MODULE MSIB	6-25
RECOMMENDATION	12	A/R	GREASE, STEM	NONE

FIGURE 6-16. MATERIAL LIST FOR MODULE ASSEMBLY



NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: NITRILE RUBBER, BUNA-N,SHORE A, 60 DUROMETER.

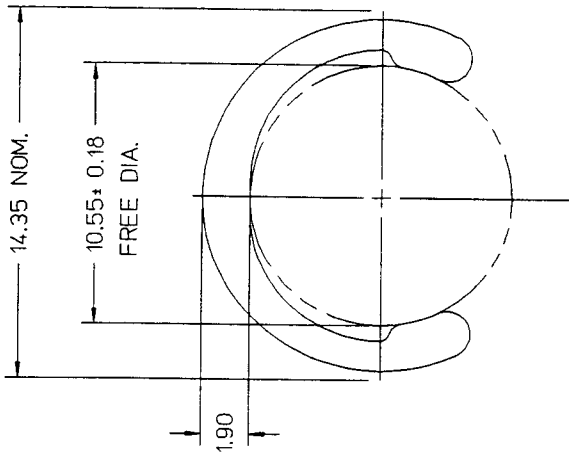
UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- THIRD ANGLE PROJECTION
- TOLERANCES

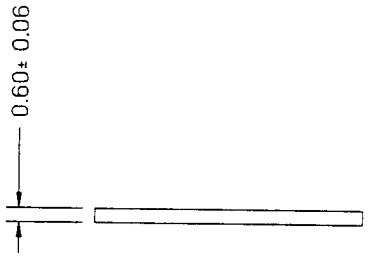
XX ~~± 0.5mm or ±~~
XX.X ~~± 0.2mm or ±~~
XX.XX ~~± 0.1mm or~~ ± 0.15
~~ALL ± _____mm~~

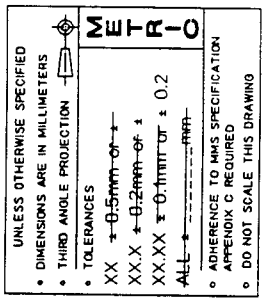
METRIC

- ADHERENCE TO MMS SPECIFICATION APPENDIX C REQUIRED
- DO NOT SCALE THIS DRAWING

FIGURE 6-17. O-RING



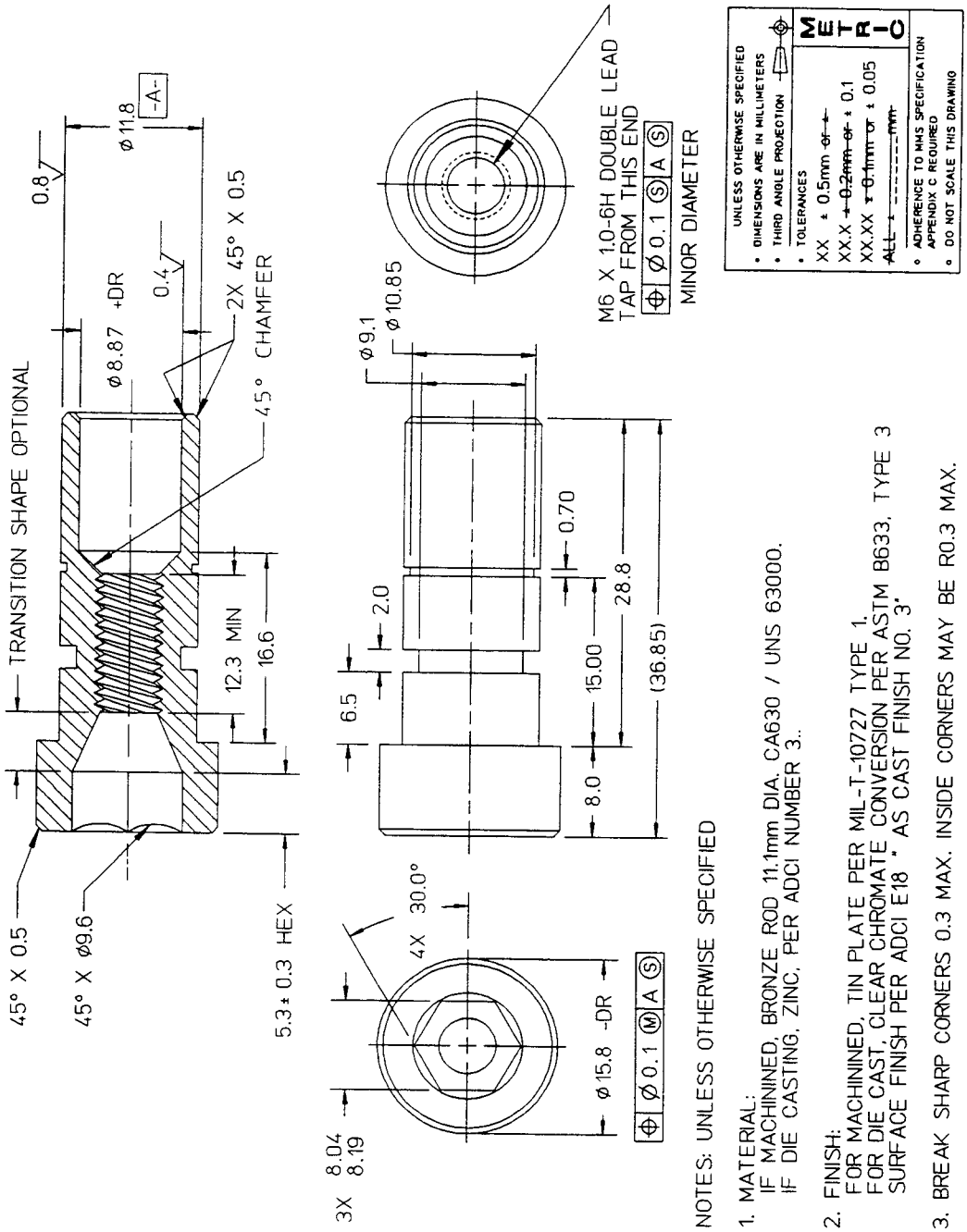




NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: CARBON SPRING STEEL, ANSI STANDARD B27.8M, TYPE 3FM1.
2. FINISH: BLACK OXIDE

FIGURE 6-18. RETAINING RING



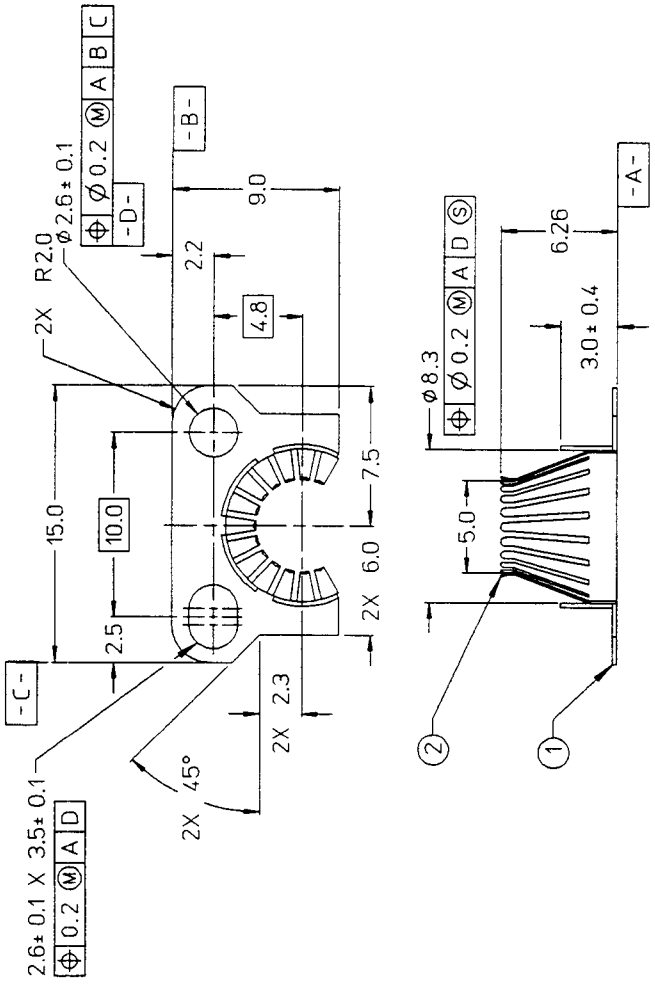
NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL:
   IF MACHINNED, BRONZE ROD 11.1mm DIA. CA630 / UNS 63000.
   IF DIE CASTING, ZINC, PER ADCI NUMBER 3.

2. FINISH:
   FOR MACHINNED, TIN PLATE PER MIL-T-10727 TYPE 1.
   FOR DIE CAST, CLEAR CHROMATE CONVERSION PER ASTM B633, TYPE 3
   SURFACE FINISH PER ADCI E18 " AS CAST FINISH NO. 3"

3. BREAK SHARP CORNERS 0.3 MAX. INSIDE CORNERS MAY BE R0.3 MAX.

FIGURE 6-19. LATCH, MODULE



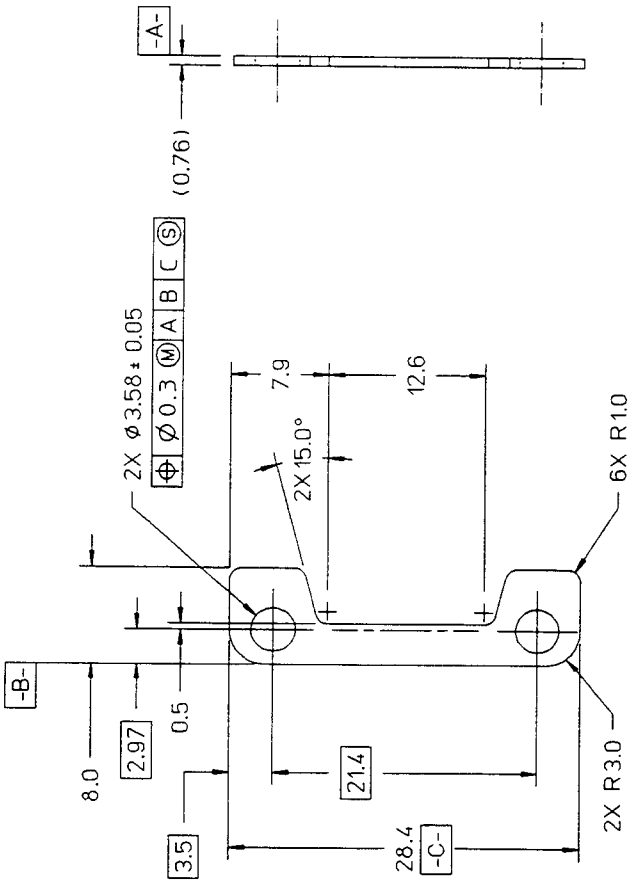
NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL:
   ITEM 1, BERYLLIUM COPPER SHEET, 0.254 mm THICK, CA172 / UNS C17200
   ITEM 2, BERYLLIUM COPPER SHEET, 0.102 mm THICK, CA172 / UNS C17200
2. FINISH:
   GOLD PLATE PER MIL-G-45204, TYPE 1, GRADE C. 2.0-3.0um THICK.
3. ASSEMBLY MAY BE SPOTWELDED OR SOLDERED.
4. BREAK SHARP CORNERS R 0.1 OR CHAMFER.

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- THIRD ANGLE PROJECTION
- TOLERANCES
  XX ~~± 0.5mm or ±~~
  XX.X ~~± 0.2mm or~~ ±0.4
  XX.XX ~~± 0.1mm or~~ ±0.2
  ALL ~~± _____ mm~~
- ADHERENCE TO MMS SPECIFICATION APPENDIX C REQUIRED
- DO NOT SCALE THIS DRAWING

METR-C

FIGURE 6-20. SPRING, GROUNDING



UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- THIRD ANGLE PROJECTION
- TOLERANCES
  XX ± 0.5mm or ±
  XX.X ~~± 0.2mm or~~ ±0.1
  XX.XX ~~± 0.1mm or~~ ±
  ~~ALL ± _____ mm~~
- ADHERENCE TO MMS SPECIFICATION APPENDIX C REQUIRED
- DO NOT SCALE THIS DRAWING

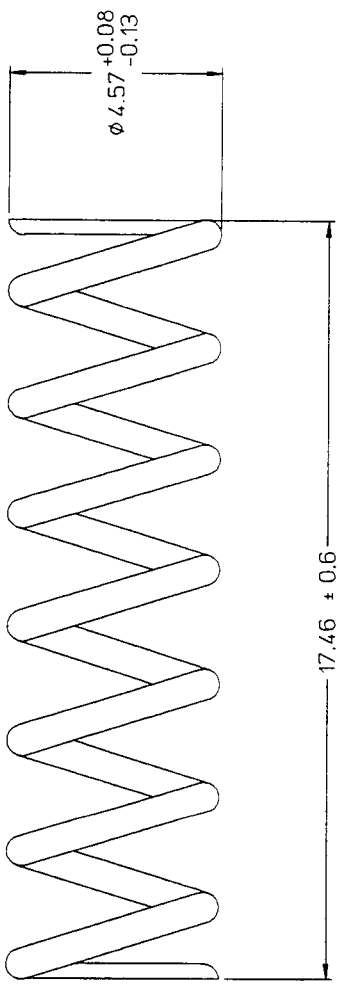
METRIC

NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: STAINLESS STEEL SHEET 0.76 ± 0.1mm THICK, AISI301 / UNS S30100, 1/2 HARD

2. FINISH: PASSIVATE PER QQ-P-35.

FIGURE 6-21. BAR, CONNECTOR



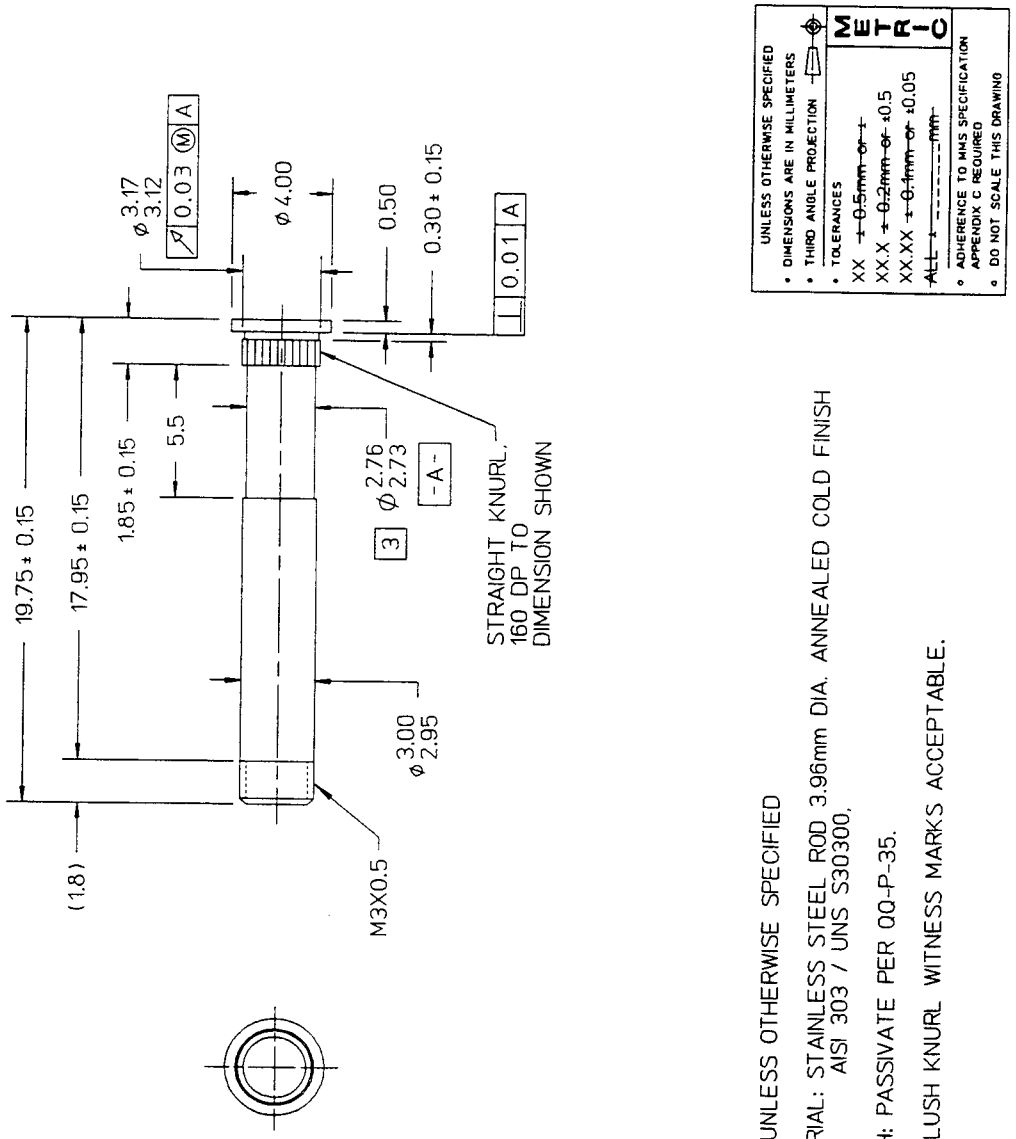
UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- THIRD ANGLE PROJECTION
- TOLERANCES
  XX
  XX.X NOTED
  XX.XX
  ALL ± _____
- ADHERENCE TO MMS SPECIFICATION APPENDIX C REQUIRED
- DO NOT SCALE THIS DRAWING

METRIC

NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: MUSIC WIRE, 0.66 mm DIA, ZINC PLATED PER QQ-W-470,ASTM A228.
2. SPRING RATE TO BE 2.8± 0.28 N/mm.
3. SQUARED AND GROUND ENDS REQUIRED.
4. STRESS RELIEF REQUIRED.

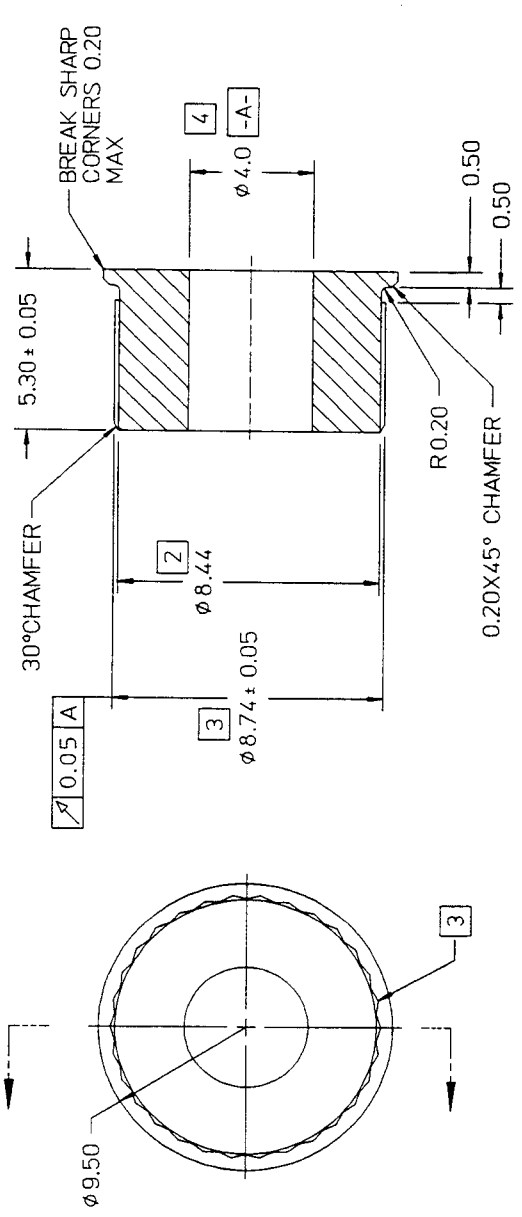
FIGURE 6-22. SPRING, COMPRESSION



NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: STAINLESS STEEL ROD 3.96mm DIA. ANNEALED COLD FINISH AISI 303 / UNS S30300.
2. FINISH: PASSIVATE PER QQ-P-35.
3. SUBFLUSH KNURL WITNESS MARKS ACCEPTABLE.

FIGURE 6-23. PIN, SPRING



UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- THIRD ANGLE PROJECTION
- TOLERANCES
  XX ± 0.5mm
  XX.X ± 0.15mm
  XX.XX ± 0.05
- ADHERENCE TO MMS SPECIFICATION APPENDIX C REQUIRED
- DO NOT SCALE THIS DRAWING

METRIC

NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: BRONZE ROD 11.1 mm DIA. CA630 / UNS 63000
2. THIS DIMENSION IS PRIOR TO KNURL OPERATION.
3. STRAIGHT KNURL, 96 DP TO DIMENSION SHOWN.
4. ⌀4.0 IS A SUGGESTION. FOR FINAL CONDITION OF PART SEE FIGURES 6-8 & 6-24.

FIGURE 6-24. BUSHING

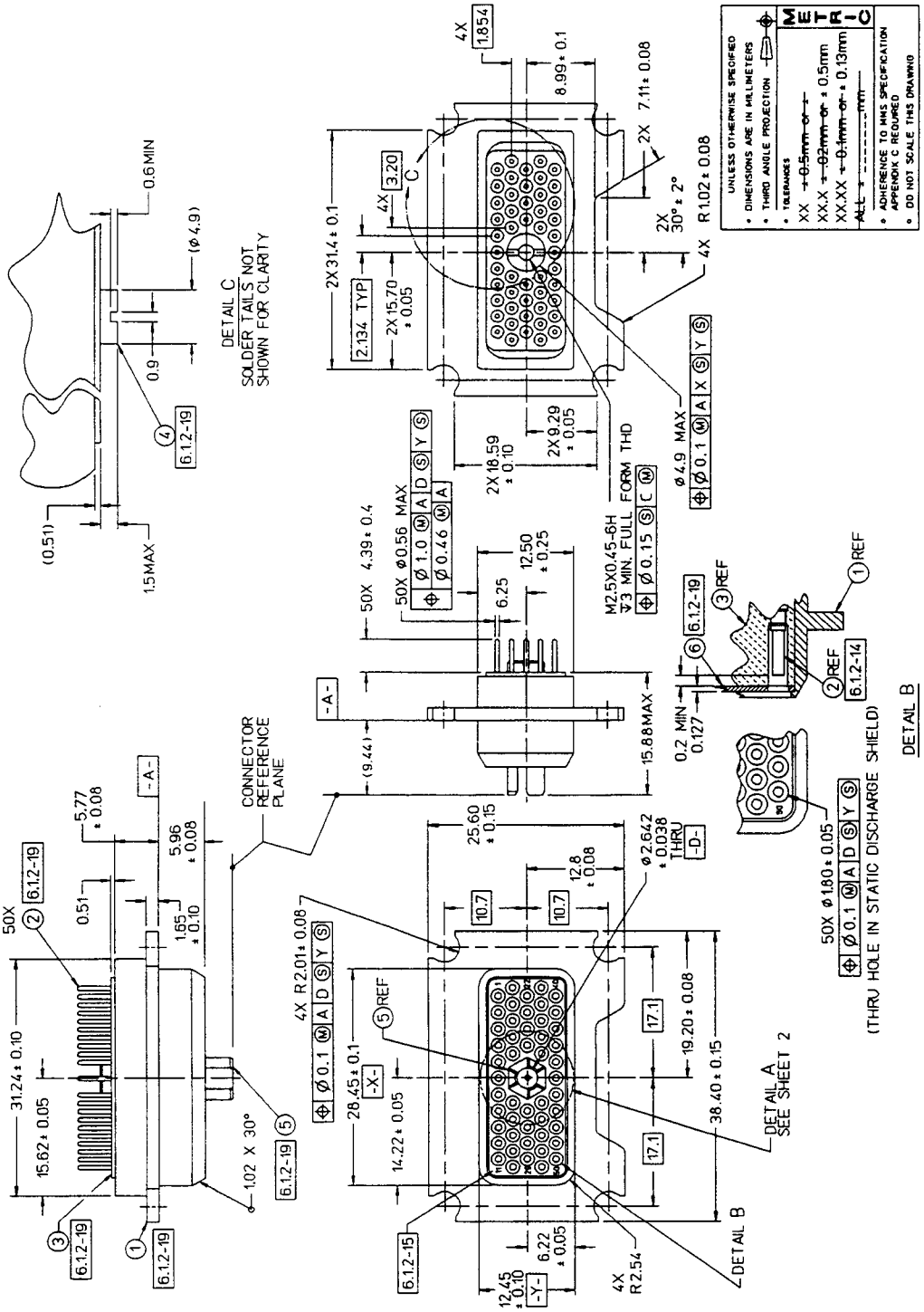
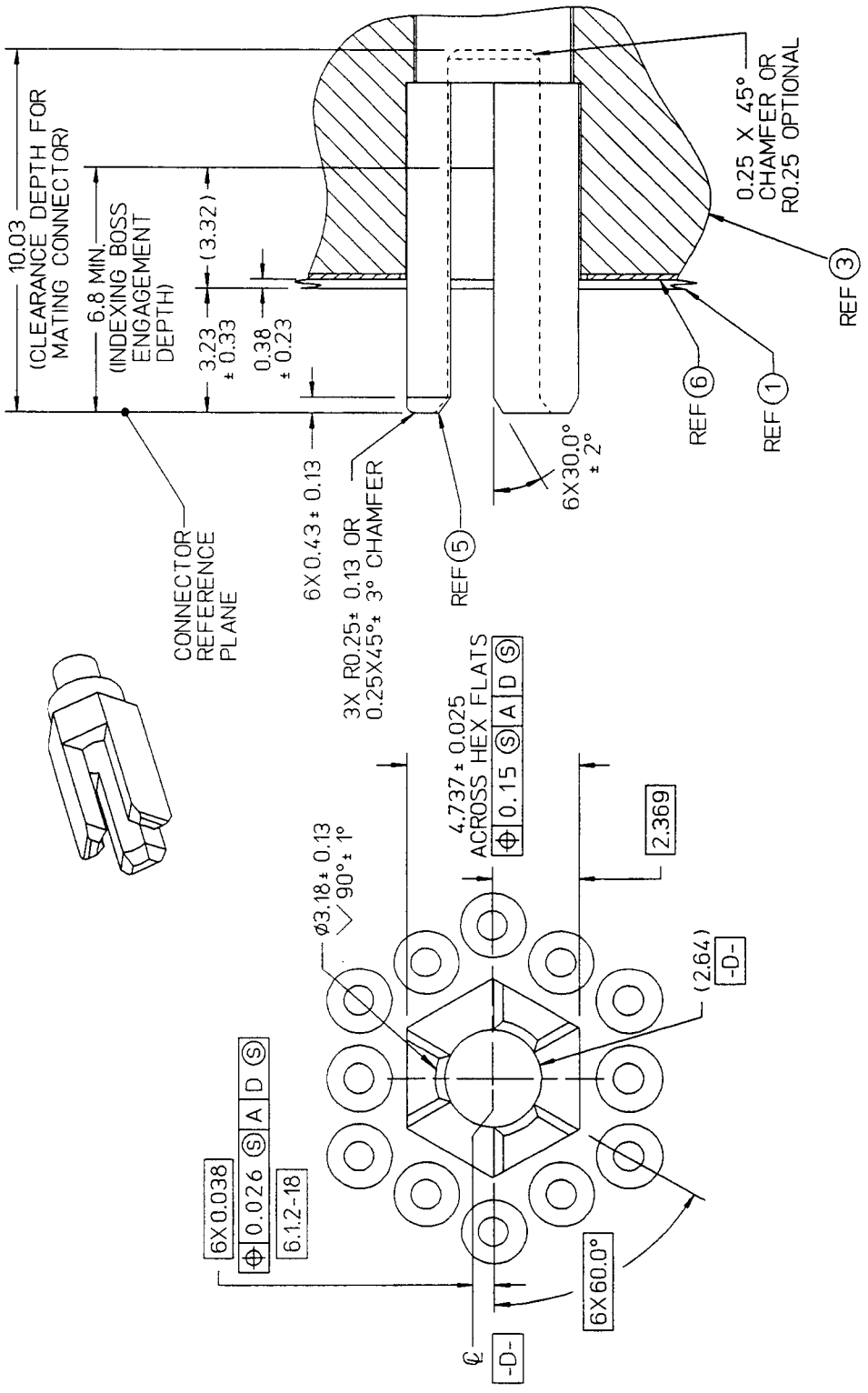


FIGURE 6-25. CONNECTOR MODULE MSB SHEET 1 OF 2



DETAIL A
INDEXING BOSS DETAIL

FIGURE 6-25 CONNECTOR, MODULE MSIB SHEET 2 OF 2

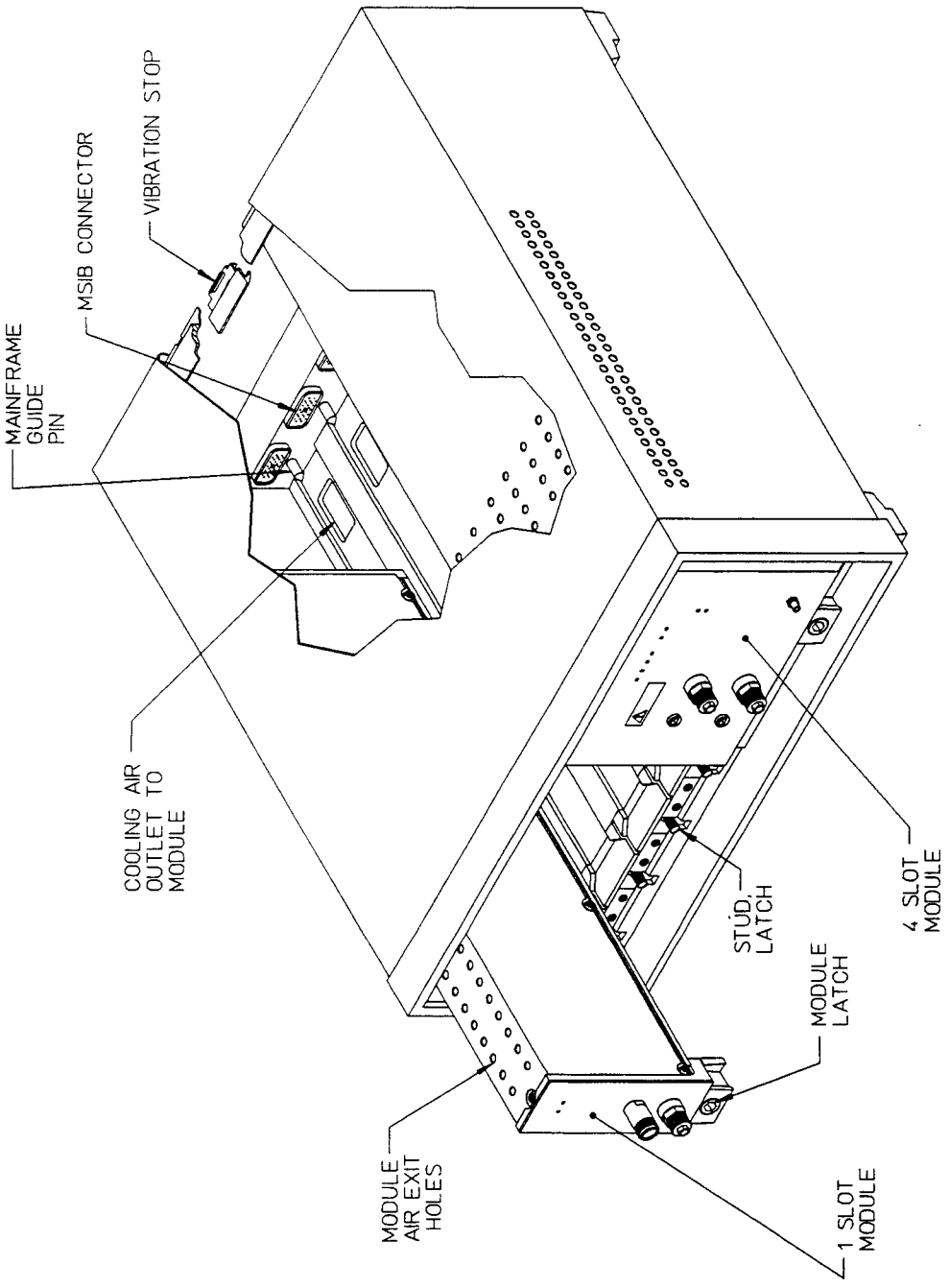


FIGURE 6-26. ISOMETRIC VIEW OF 8 SLOT MAINFRAME

MAINFRAME DATUM ORIGINS AND EXPLANATIONS

	DATUM	ORIGIN	FUNCTION
1.	-A-	MAINFRAME FRONT FACE (FIGURE 6-29)	PRIMARY DATUM FOR FRONT DETAILS.
2.	-B-	MAINFRAME FRONT 'V' FEATURE (FIGURE 6-29)	SECONDARY DATUM FOR FRONT DETAILS
3.	-C-	MAINFRAME FRONT LOCATION TAB (FIGURE 6-30)	TERTIARY DATUM FOR FRONT DETAILS.
4.	-D-	MAINFRAME GUIDE PIN (FIGURE 6-31)	TERTIARY DATUM FOR REAR DETAILS.
5.	-E-	MAINFRAME REAR FACE (FIGURE 6-31)	PRIMARY DATUM FOR REAR DETAILS.
6.	F-G	MAINFRAME GUIDE PIN PLANE (FIGURE 6-32)	SECONDARY DATUM FOR REAR DETAILS.

FIGURE 6-27. EXPLANATIONS OF MAINFRAME DATUMS

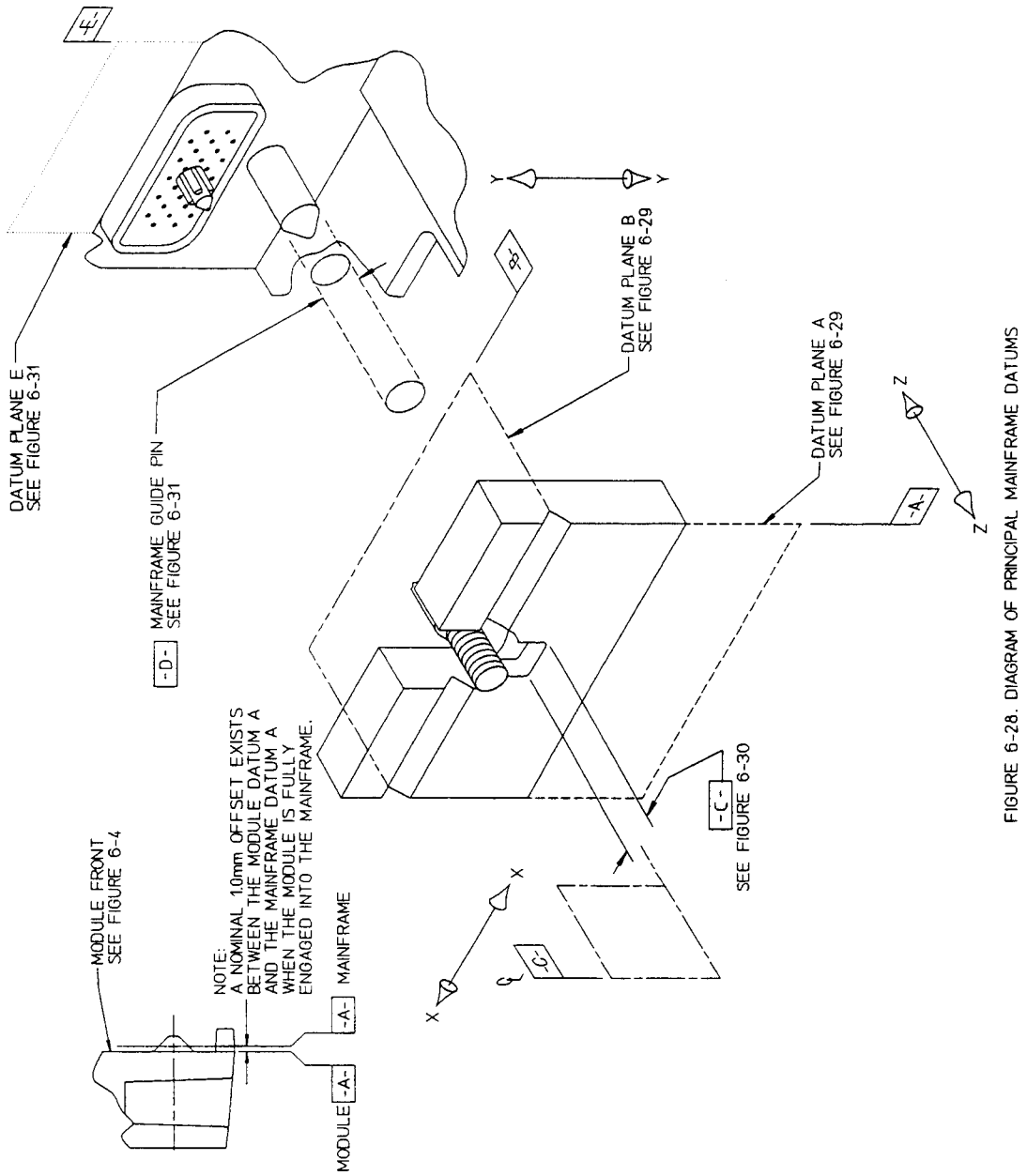


FIGURE 6-28. DIAGRAM OF PRINCIPAL MAINFRAME DATUMS

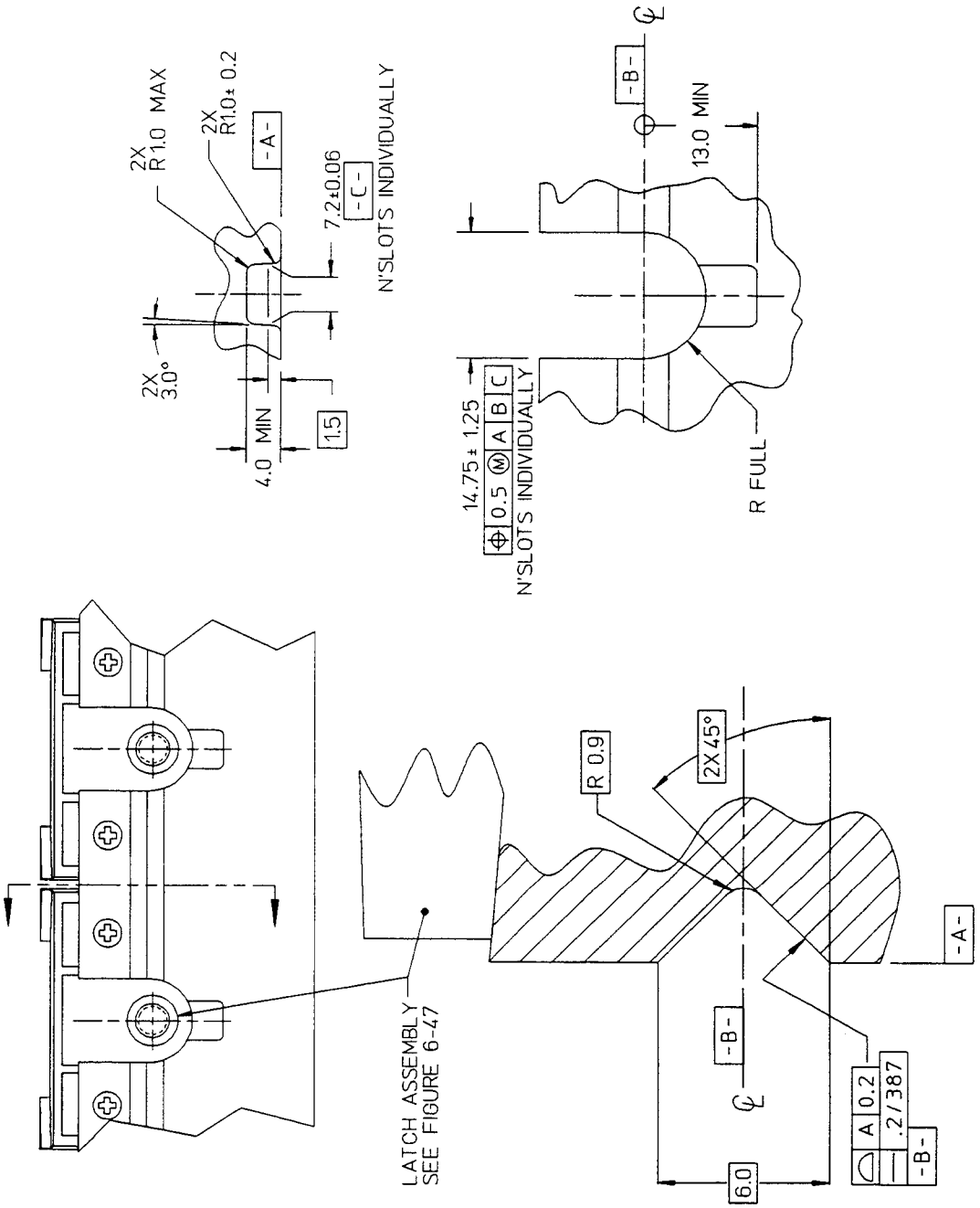


FIGURE 6-29. DETAIL OF MAINFRAME DATUM A & B

FIGURE 6-30. DETAIL OF MAINFRAME DATUM C

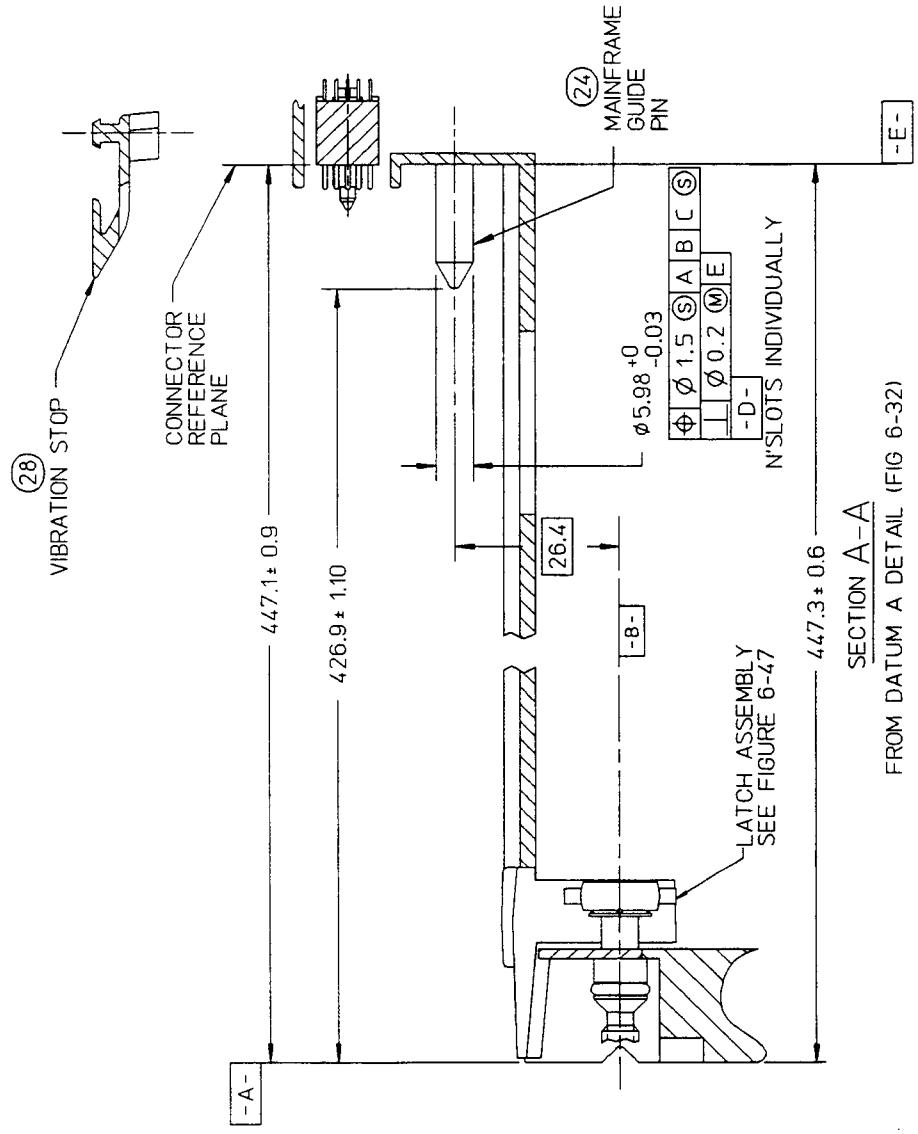


FIGURE 6-31. DETAIL OF MAINFRAME DATUM D & E

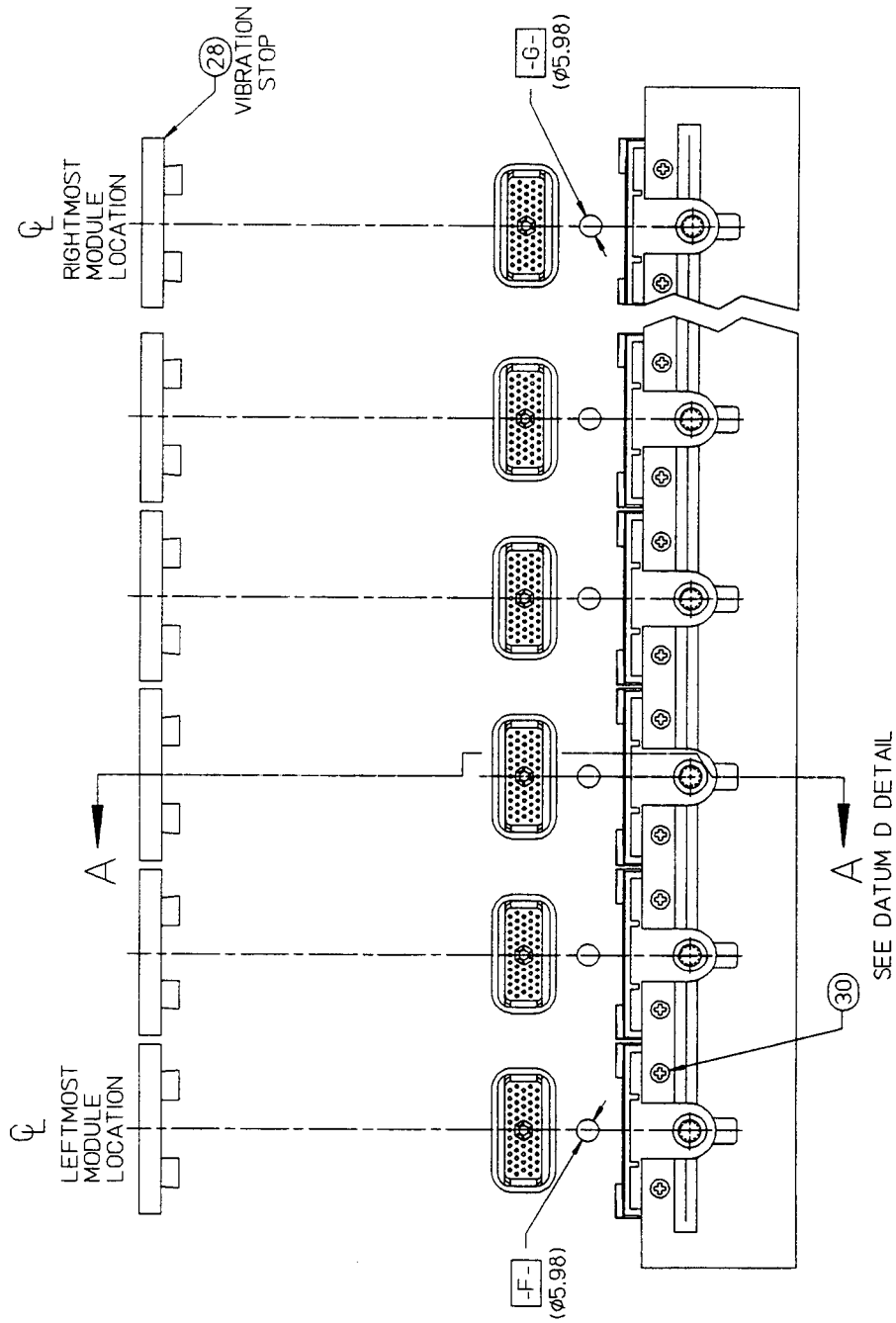


FIGURE 6-32. DETAIL OF MAINFRAME DATUM F-G

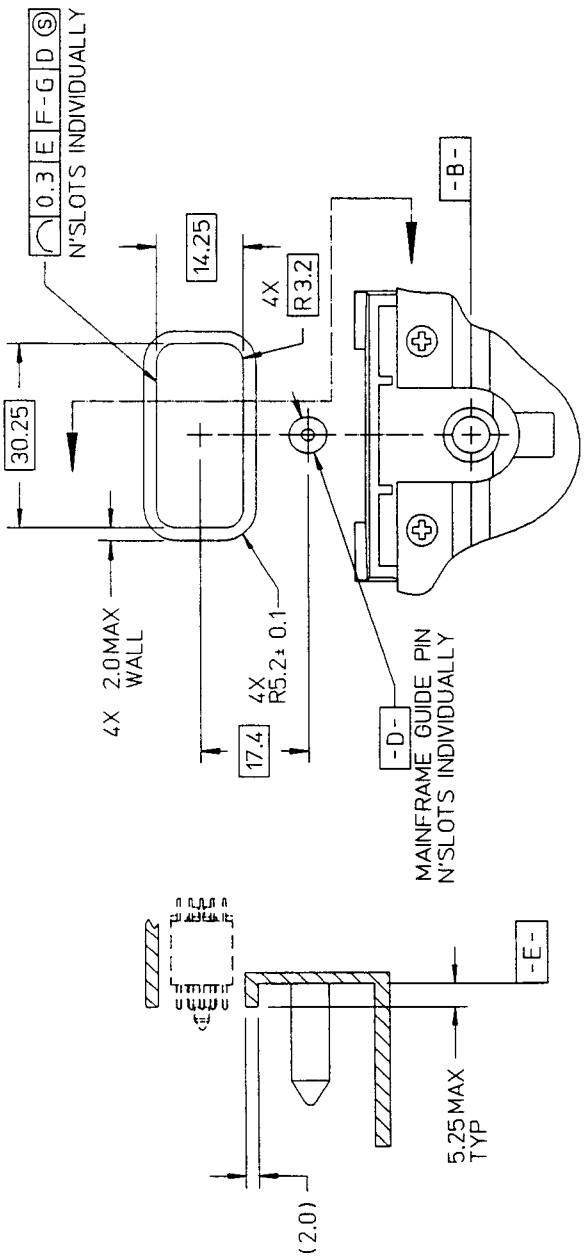


FIGURE 6-33. DETAIL OF MAINFRAME CONNECTOR HOOD

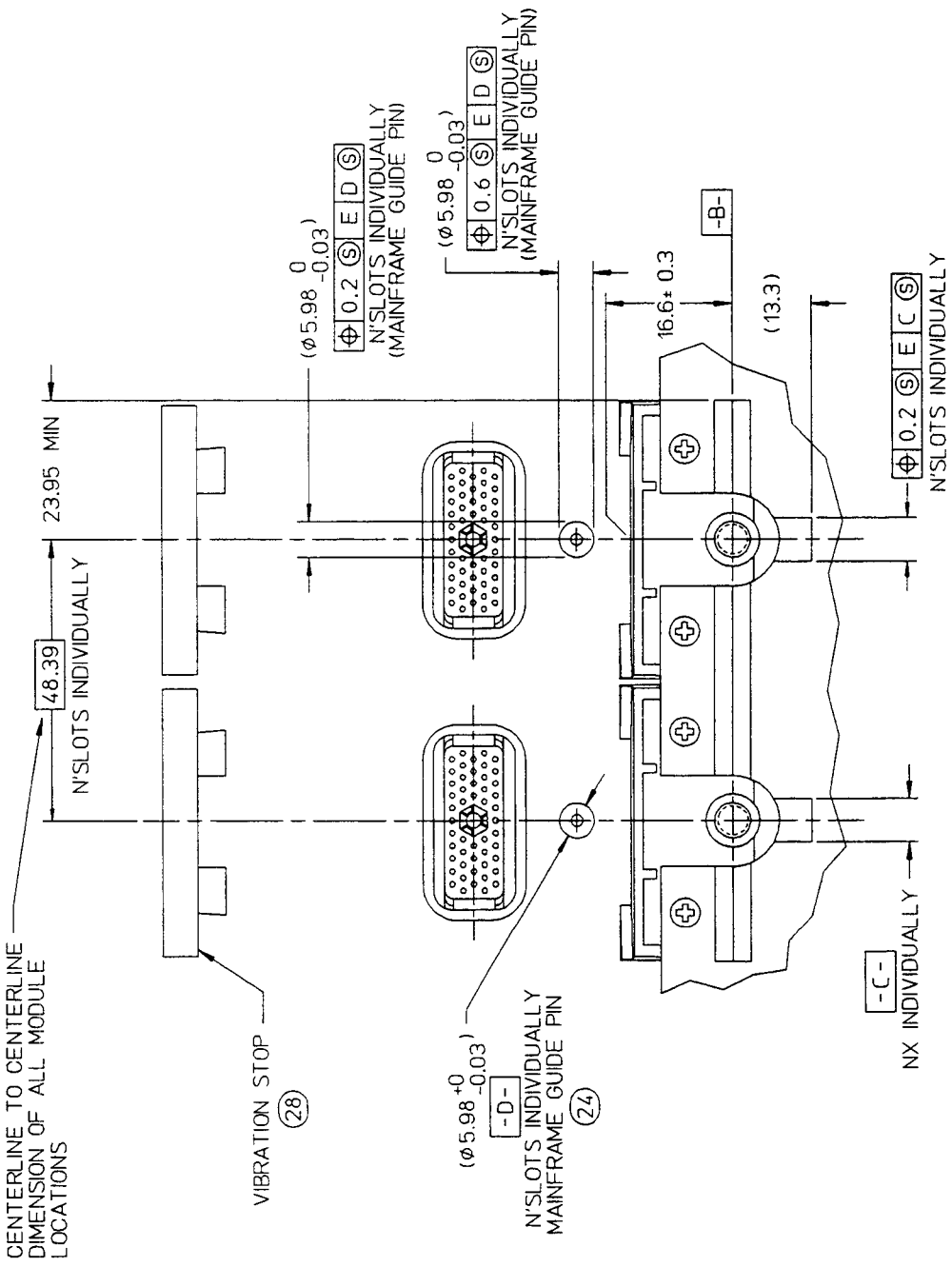


FIGURE 6-34. RELATIONSHIP BETWEEN MAINFRAME SLOTS

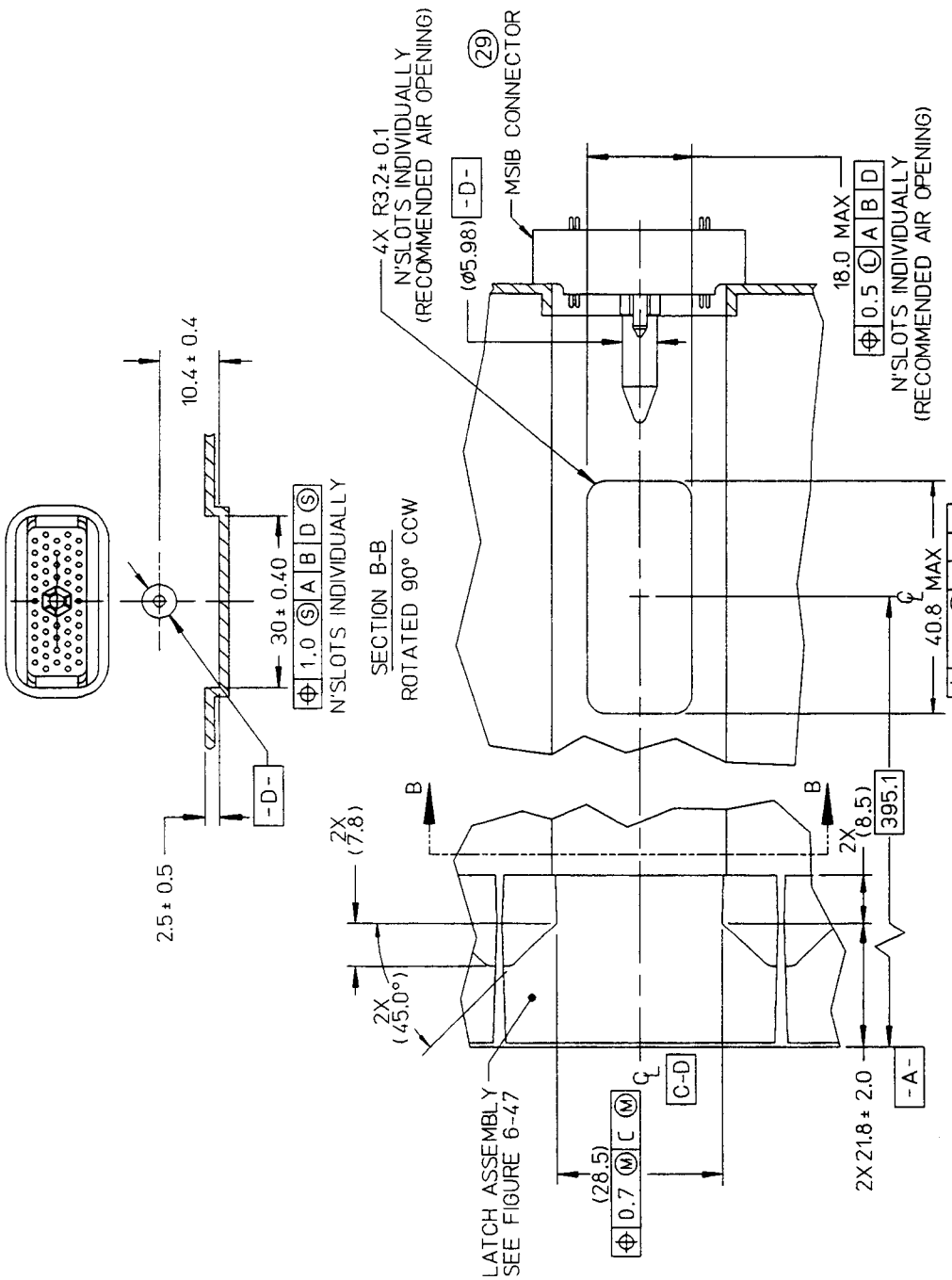


FIGURE 6-35. MAINFRAME CHANNEL DETAIL, TOP VIEW

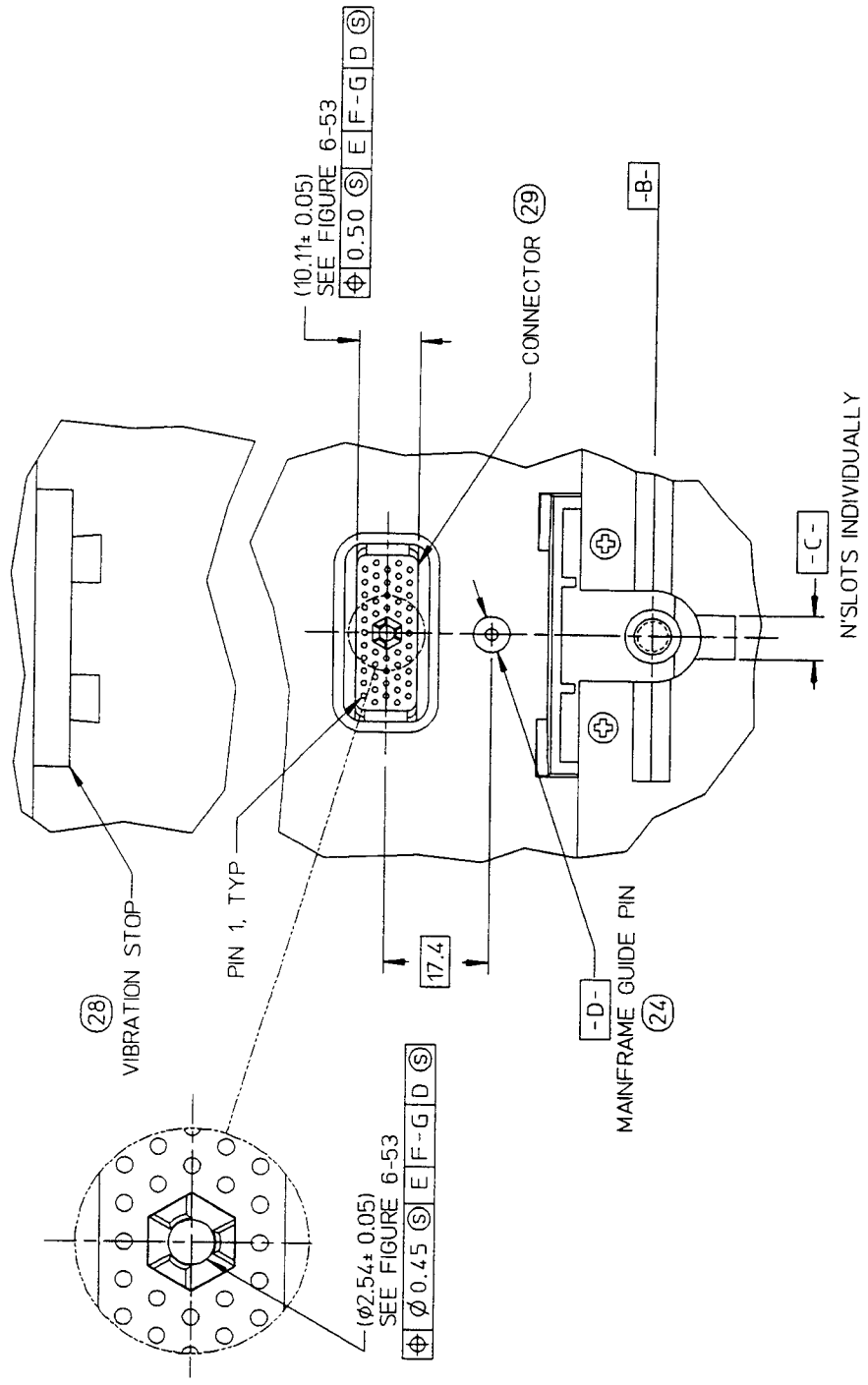


FIGURE 6-36. MAINFRAME SLOT DETAIL, FRONT TO REAR VIEW

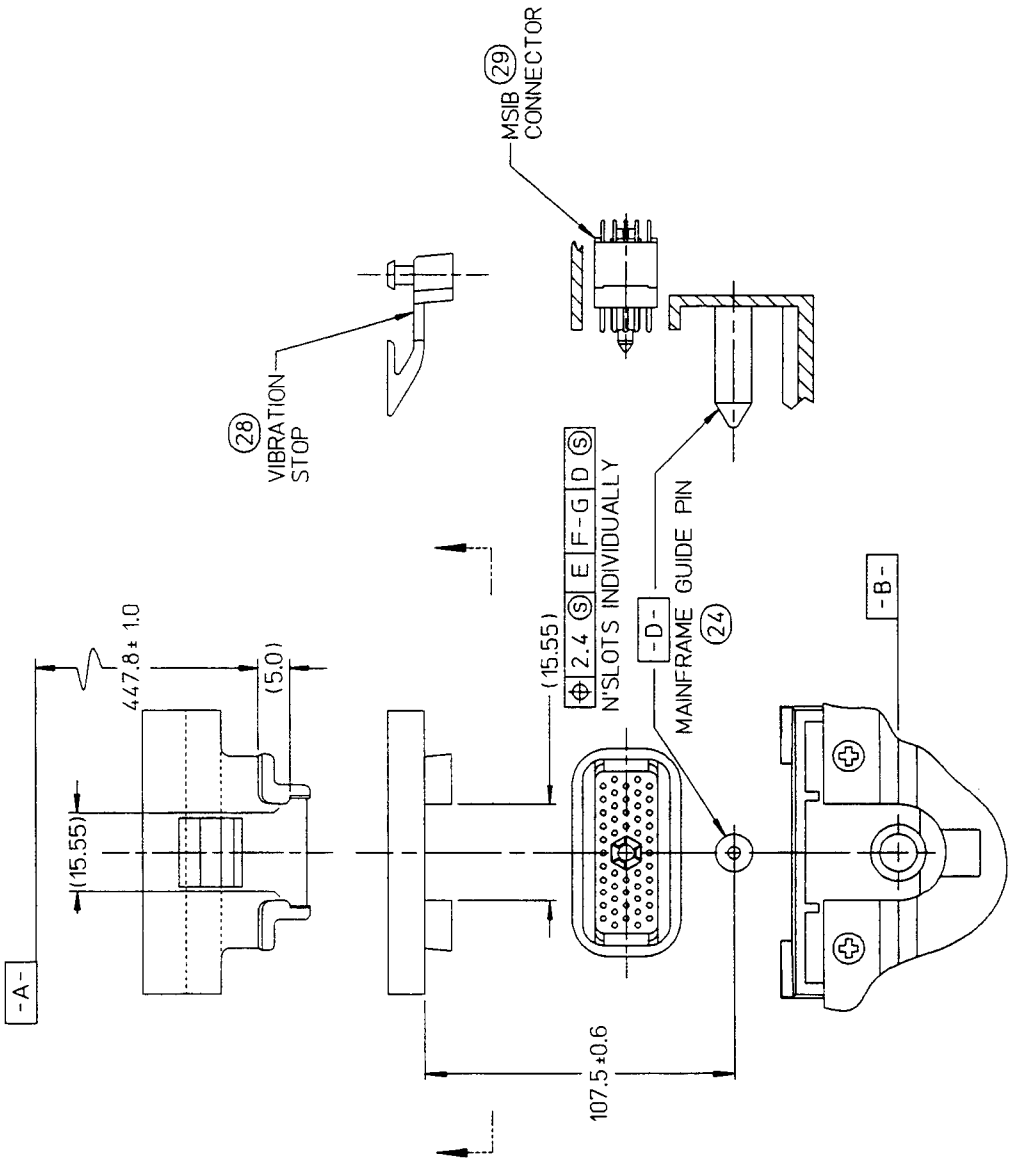


FIGURE 6-37. VIBRATION STOP PARAMETERS

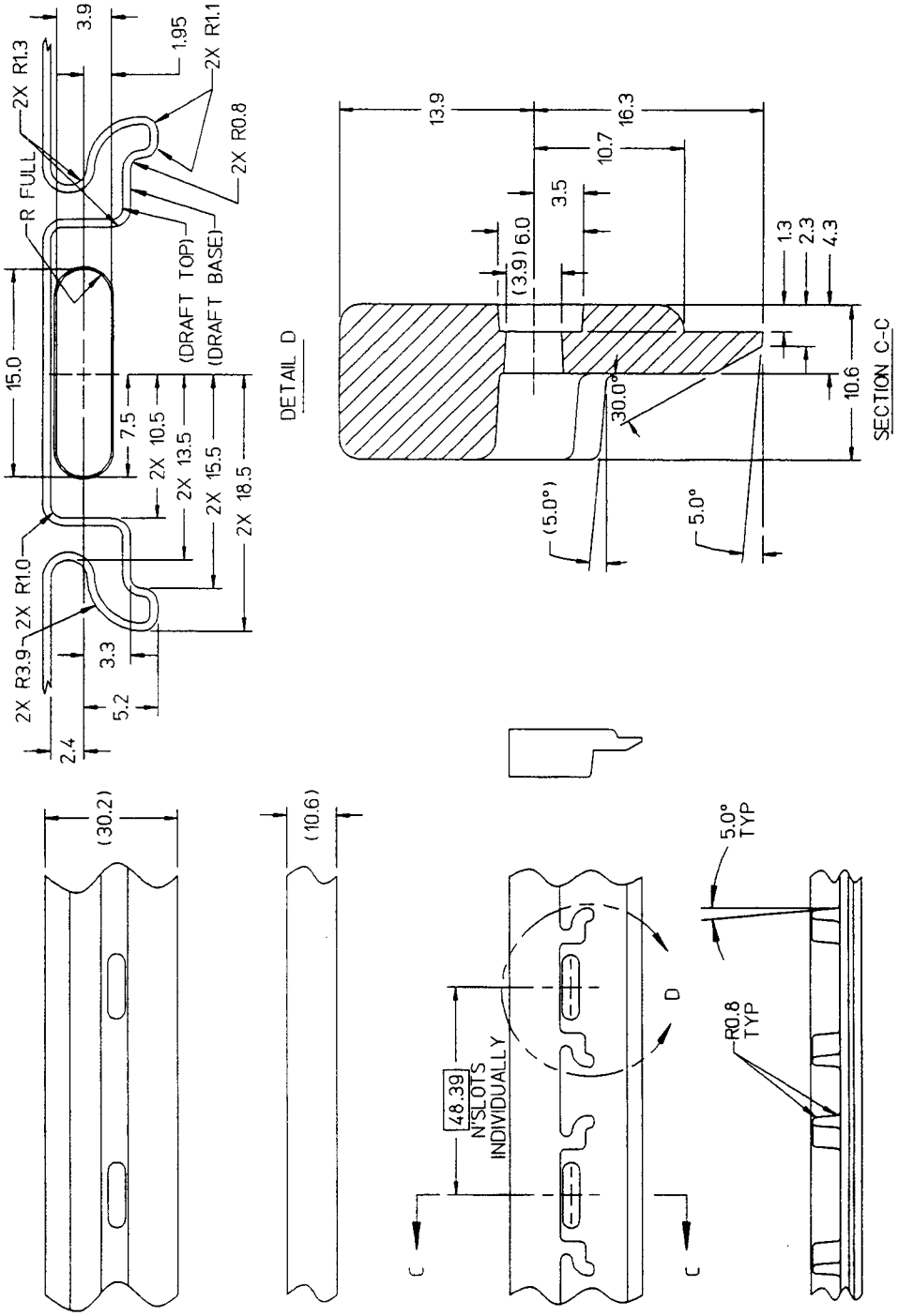


FIGURE 6-38. VIBRATION STOP RETAINER

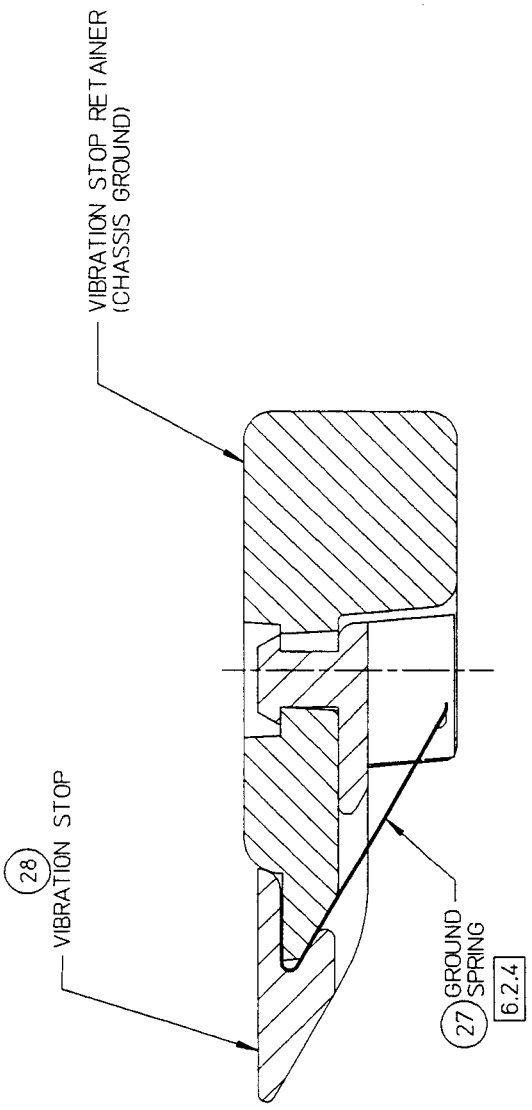


FIGURE 6-39. VIBRATION STOP ASSEMBLY

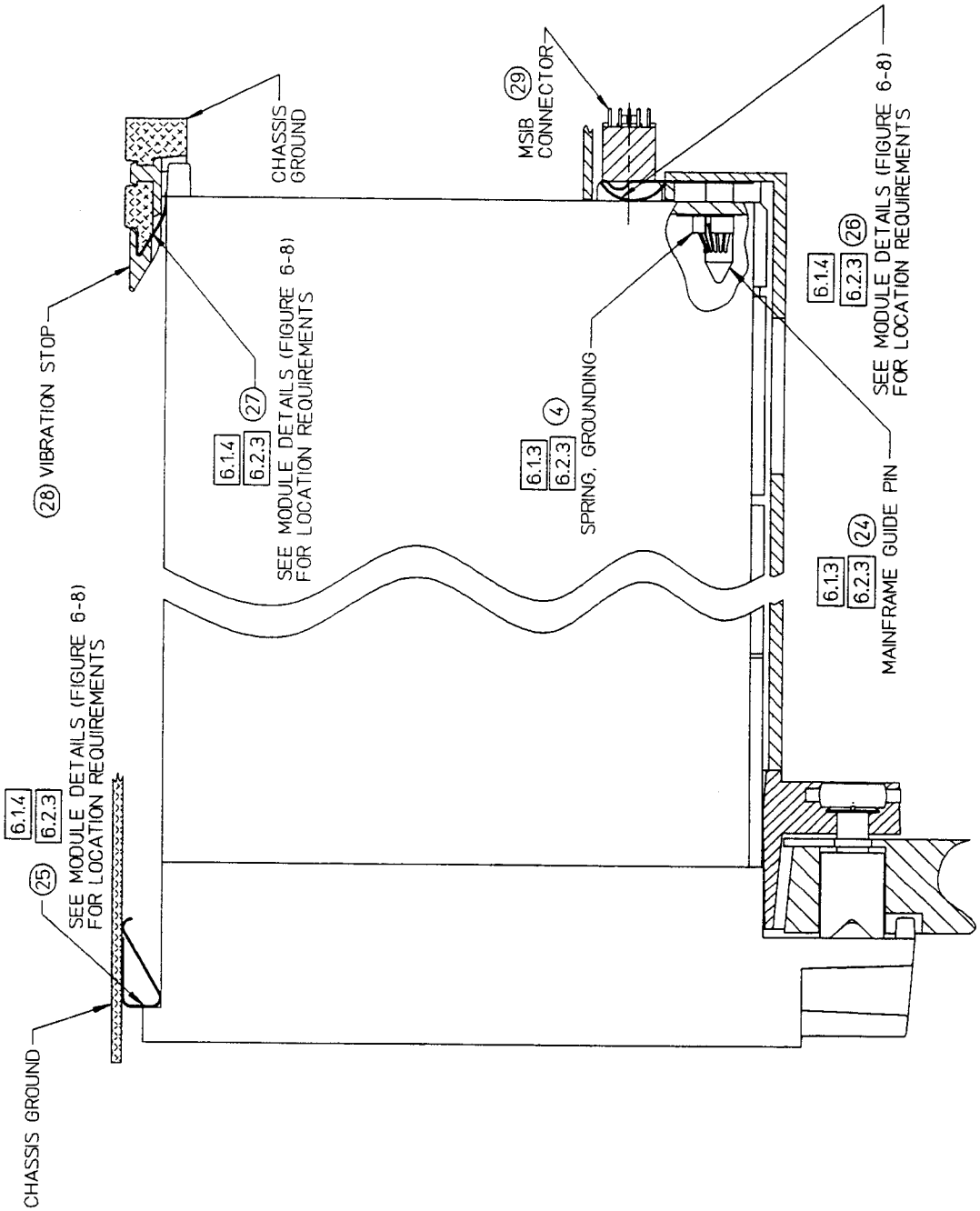


FIGURE 6-40. GROUND SPRING ASSEMBLY DETAIL

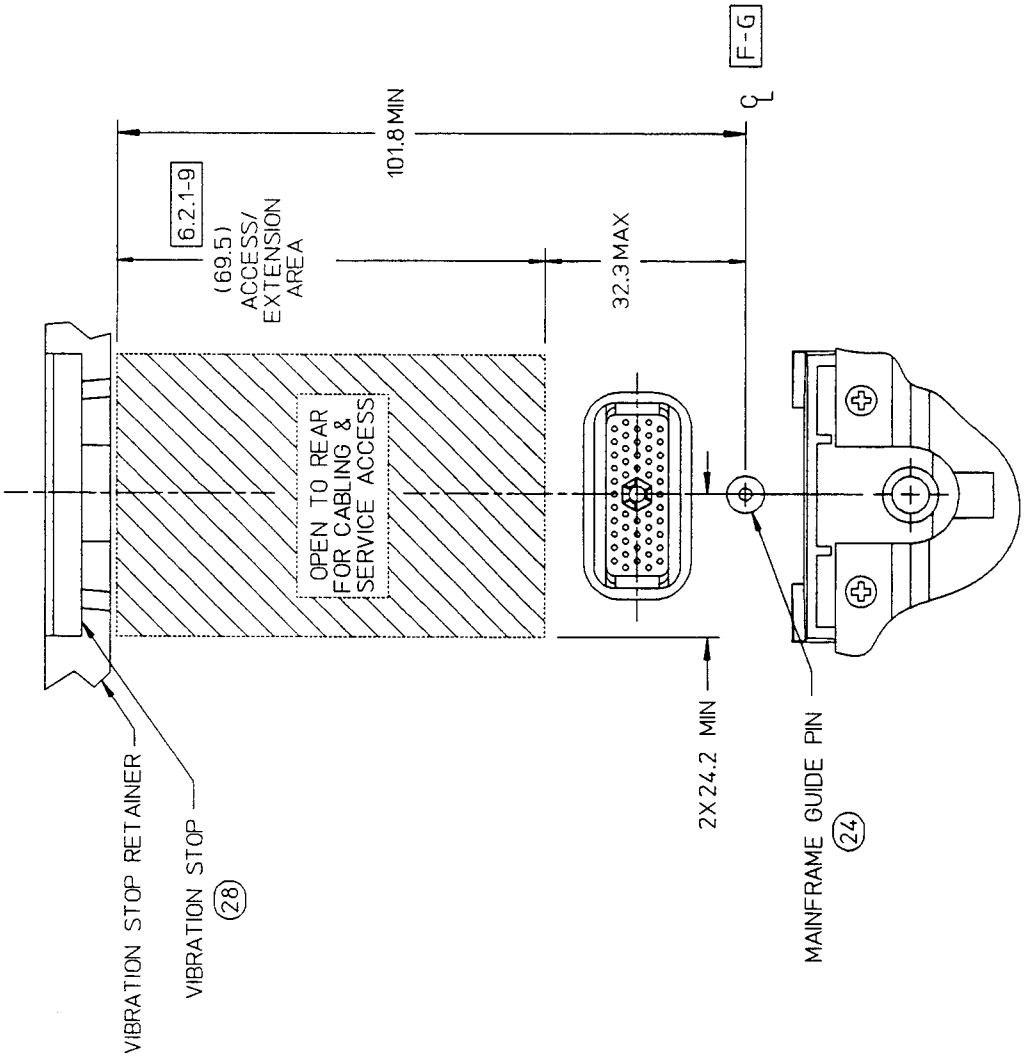


FIGURE 6-41. MAINFRAME SLOT REAR PANEL ACCESS

MATERIAL LIST FOR MAINFRAME ASSEMBLY

	ITEM	QTY	MAT'L DESCRIPTION	FIG. #
RULE	20	1 PER SLOT	STUD, LATCH	6-43
RULE	21	1 PER SLOT	HOUSING, LATCH	6-44
RULE	22	1 PER SLOT	SPRING, LATCH	6-45
RULE	23	1 PER SLOT	RETAINER, LATCH	6-46
RULE	24	1 PER SLOT	PIN, MAINFRAME GUIDE	6-48
SUGGESTION	25	1 PER 4 SLOTS	GROUND SPRING, TOP FRONT	6-49
SUGGESTION	26	1 PER 4 SLOTS	GROUND SPRING, BOTTOM REAR	6-51
SUGGESTION	27	1 PER SLOT	GROUND SPRING, TOP REAR	6-50
RECOMMENDATION	28	1 PER SLOT	VIBRATION STOP	6-52
RULE	29	1 PER SLOT	CONNECTOR, MAINFRAME	6-53
RECOMMENDATION	30	2 PER SLOT	SCREW, FLAT HEAD, M3.0X25L	NONE
RULE	1	1 PER SLOT	O-RING	6-17
RECOMMENDATION	12	A/R	GREASE, STEM	NONE

FIGURE 6-42. MATERIAL LIST FOR MAINFRAME ASSEMBLY

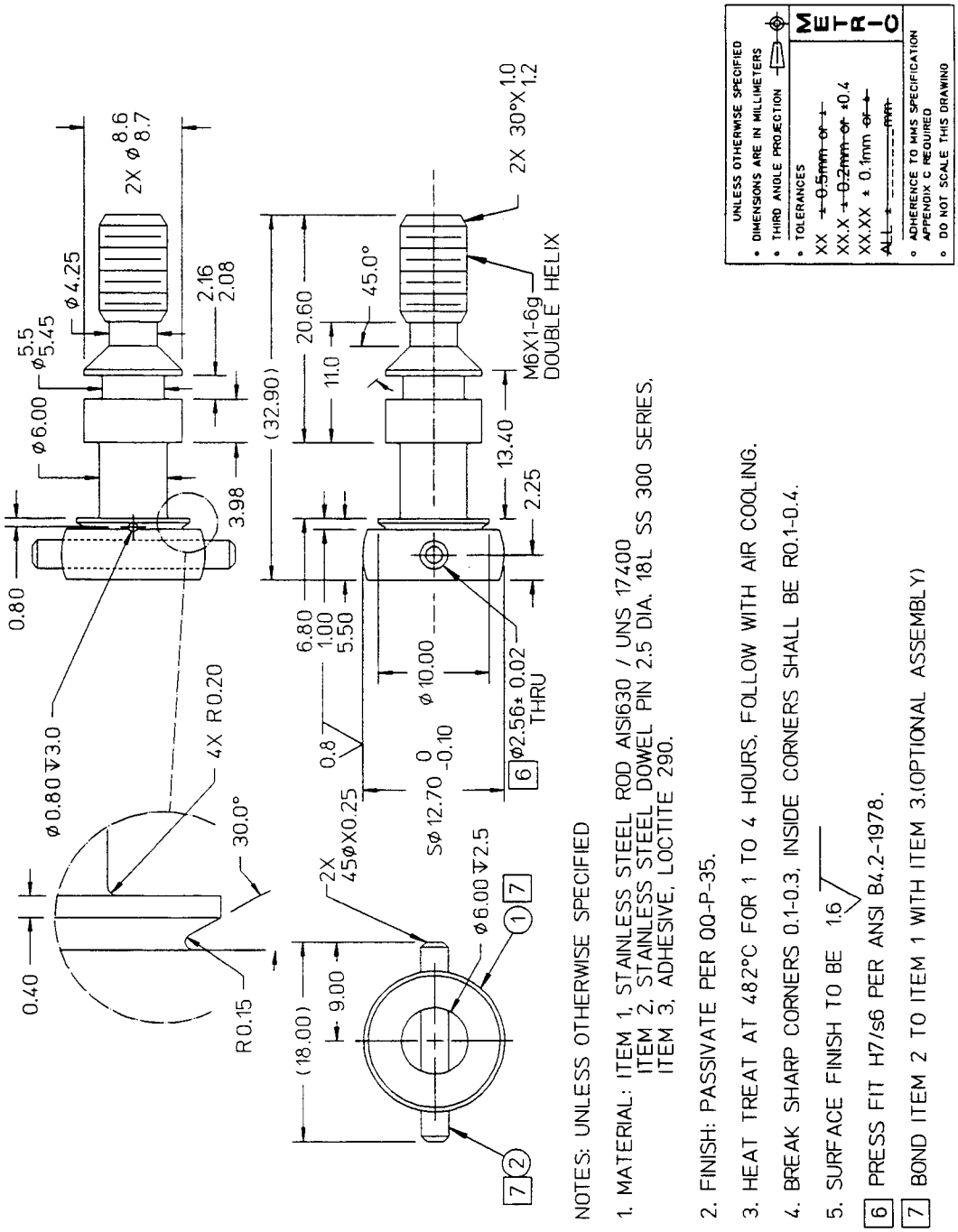


FIGURE 6-43, STUD,LATCH

NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: ITEM 1, MOLDING COMPOUND, POLYCARBONATE, 30% GLASS FIBER, 15% TFE, BLACK.
ITEM 2, INSERT, M3.0 X 0.5.

[2] FINISH: TEXTURE TO BE OBTAINED FROM MOLD WITH SPI-SPE FINISH NO.3 WHERE INDICATED, ALL OTHER SURFACES TO BE FINISHED AT MOLD MAKERS OPTION.

3. DRAFT TO BE 1.5°.

4. ALL RADII TO BE 1.0.

[5] SURFACE TO BE FREE OF EJECTOR PIN MARKS.

6. NOMINAL WALL THICKNESS TO BE 1.5.

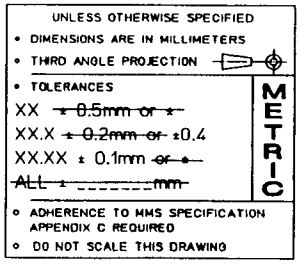


FIGURE 6-44, HOUSING, LATCH SHEET 1 OF 4

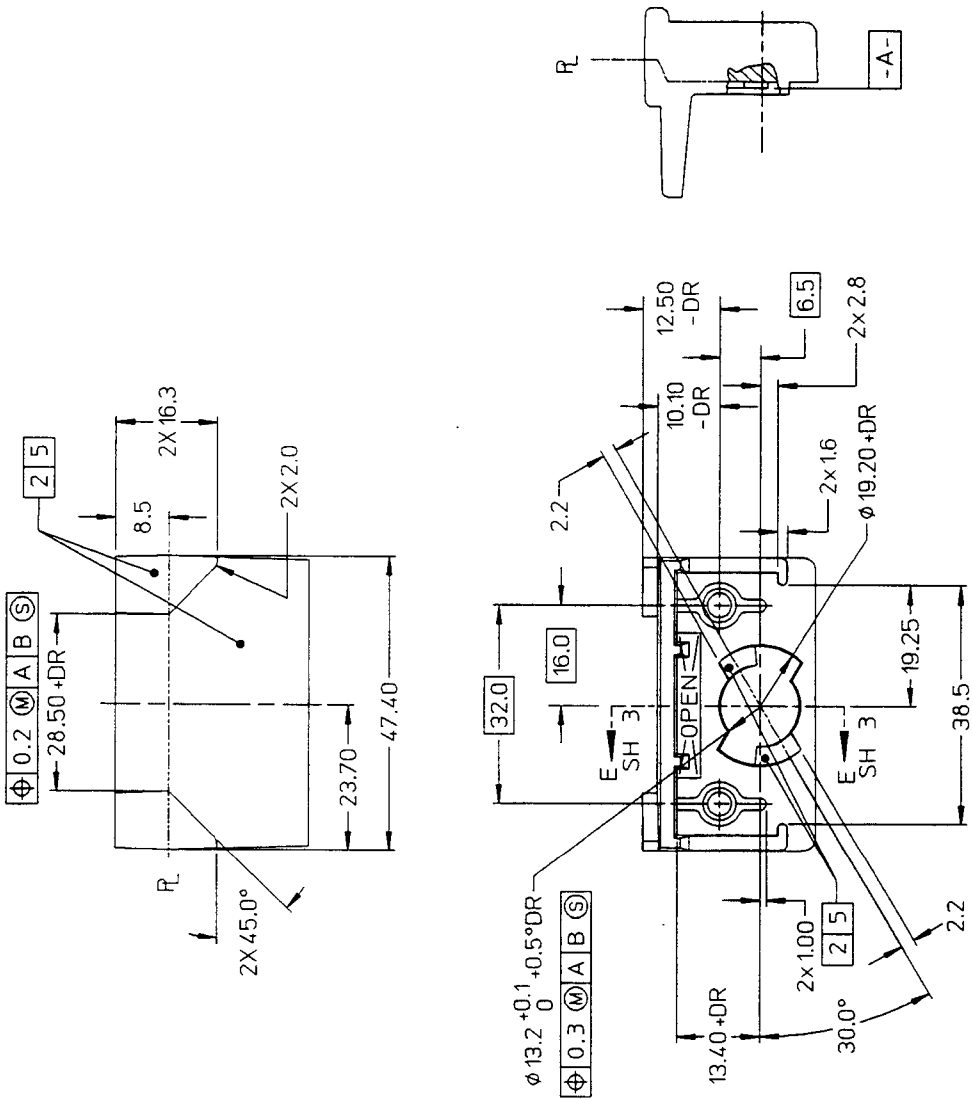


FIGURE 6-44, HOUSING, LATCH SHEET 2 OF 4

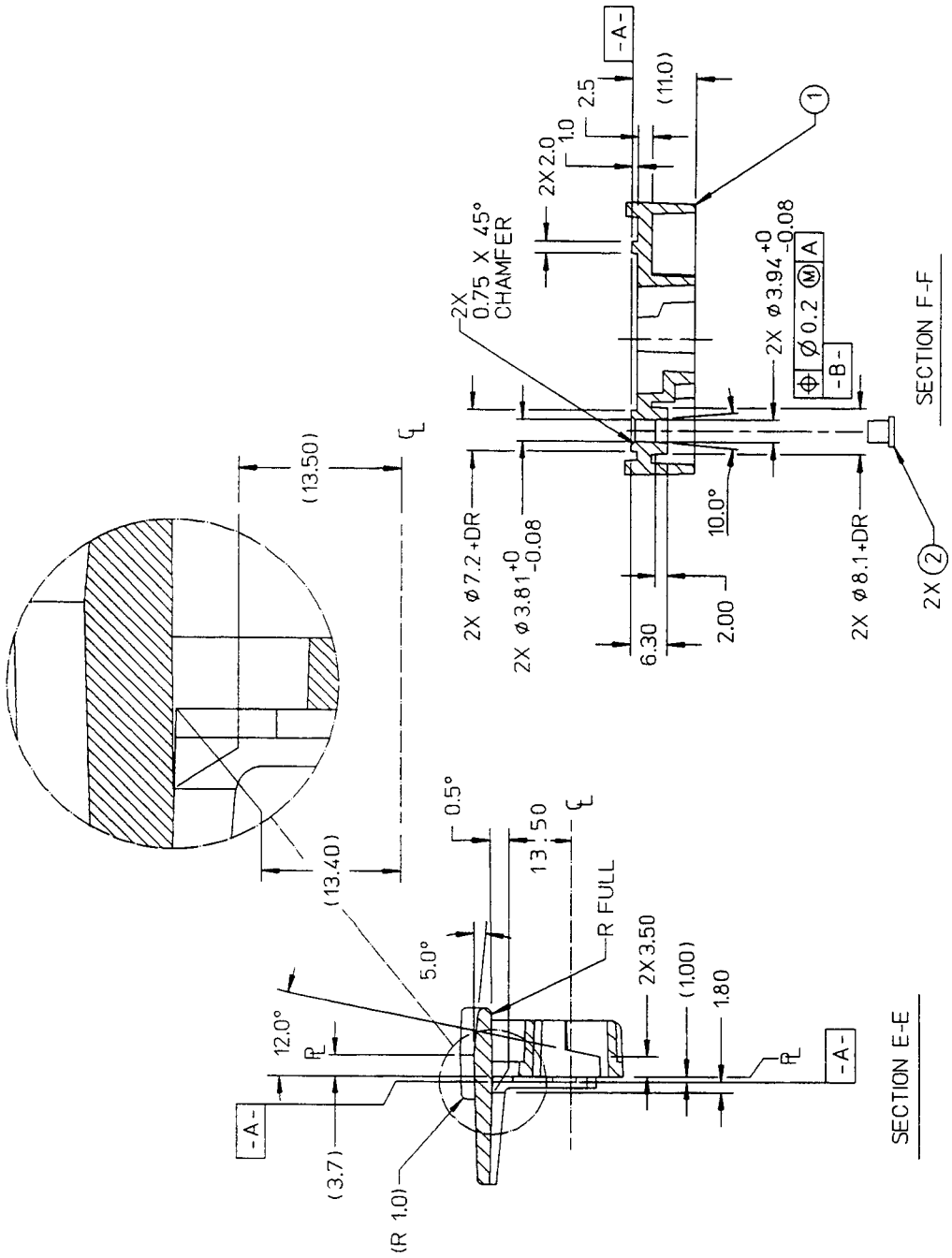


FIGURE 6-44, HOUSING, LATCH SHEET 3 OF 4

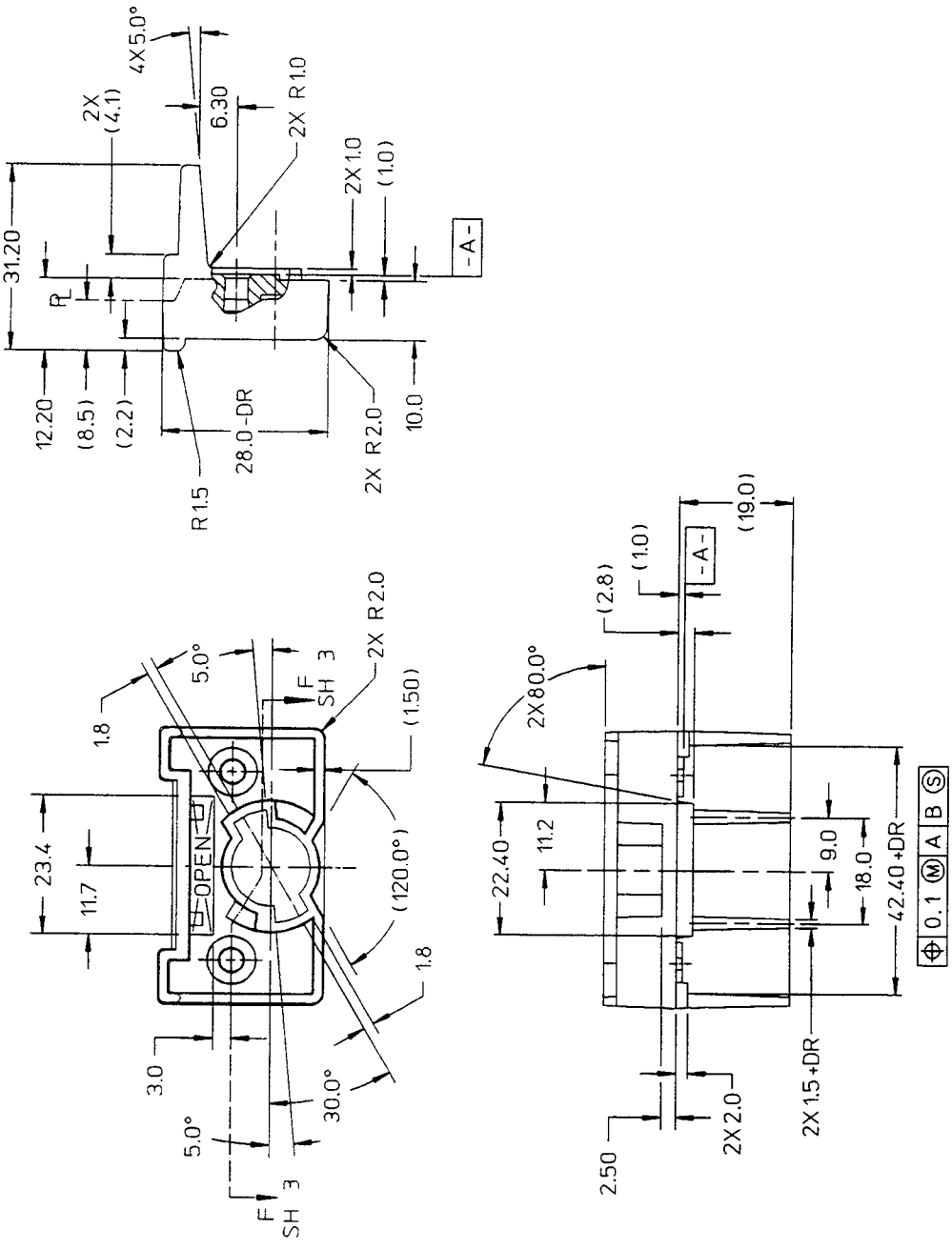
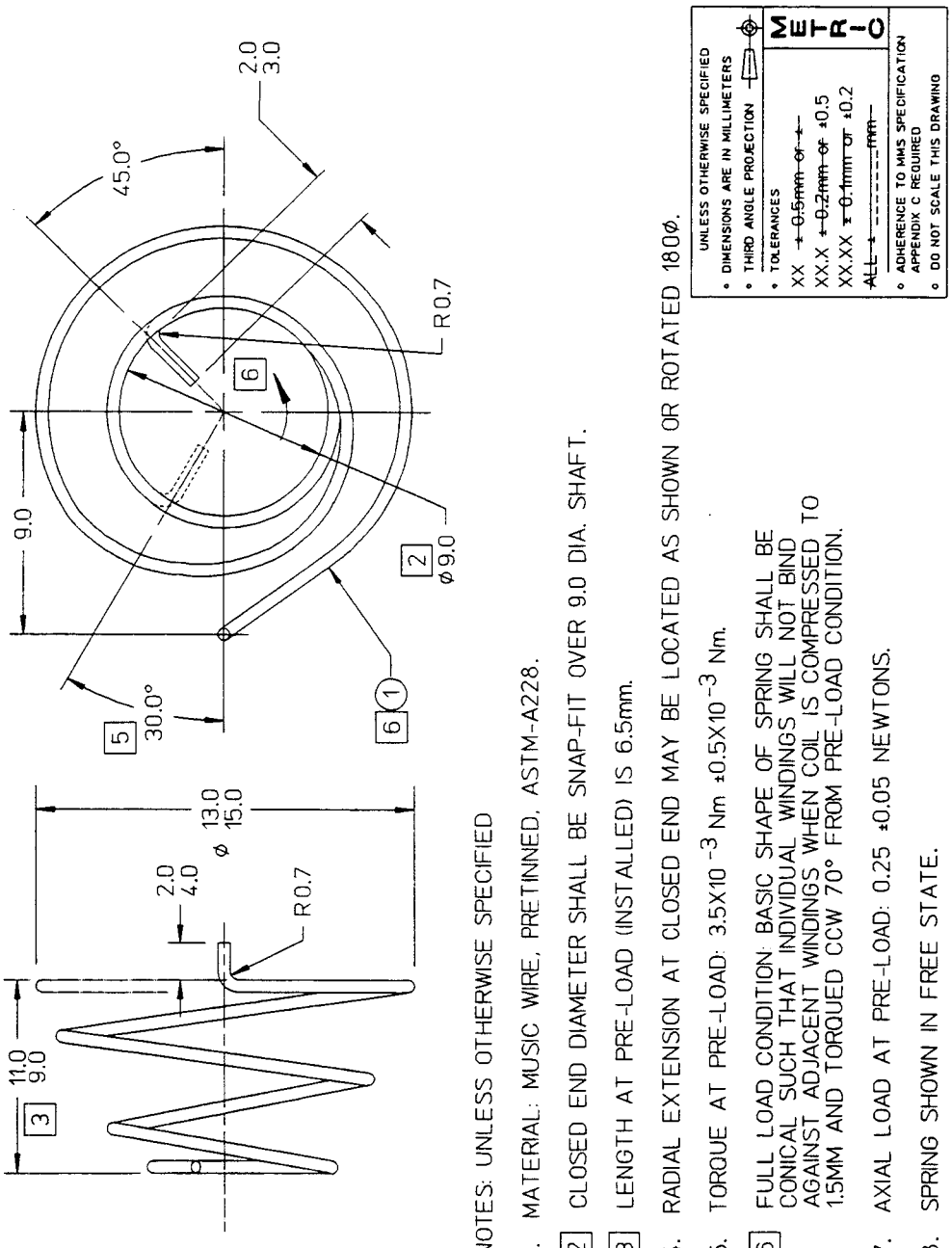


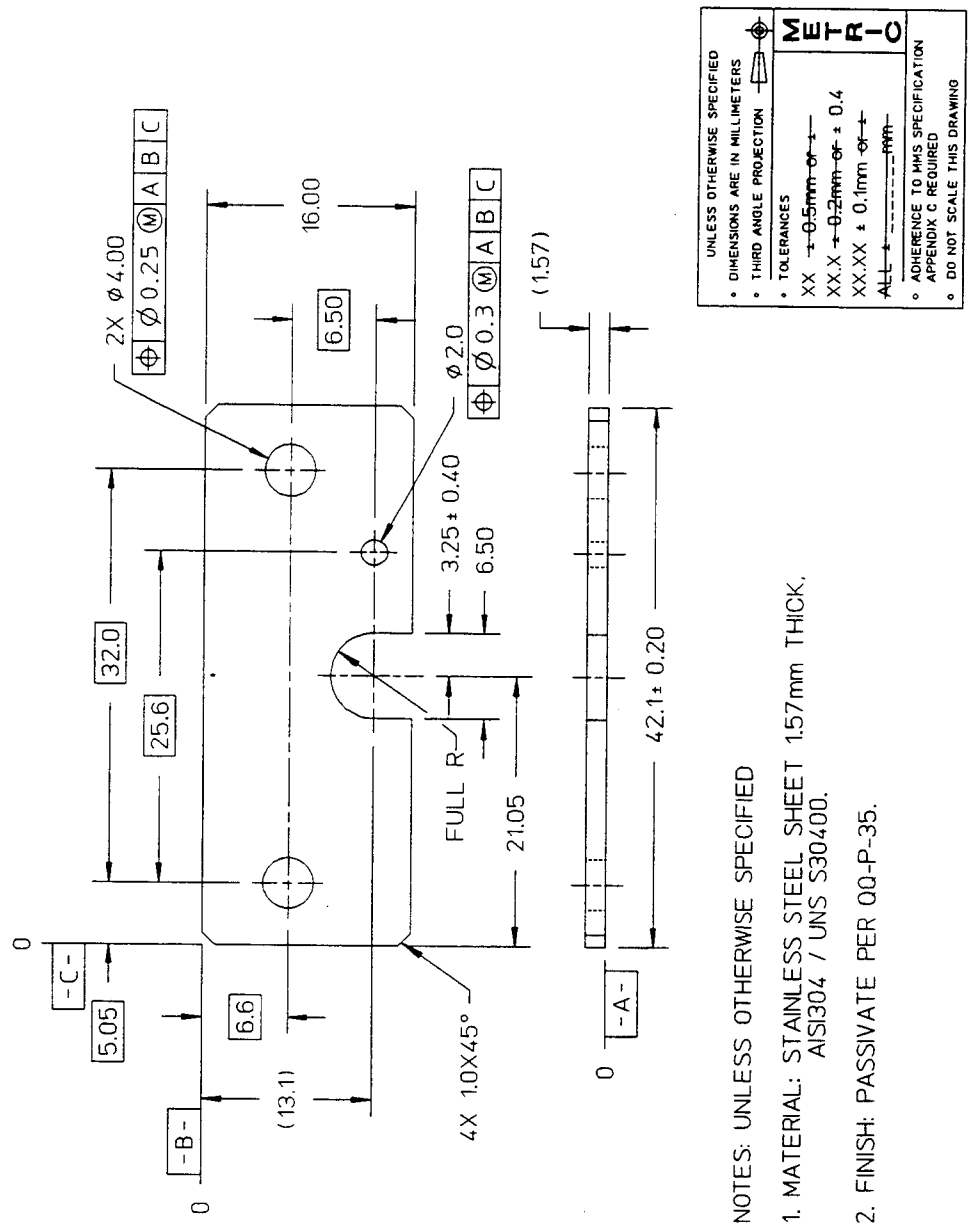
FIGURE 6-44, HOUSING, LATCH SHEET 4 OF 4



NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: MUSIC WIRE, PRETINNED, ASTM-A228.
2. [2] CLOSED END DIAMETER SHALL BE SNAP-FIT OVER 9.0 DIA. SHAFT.
3. [3] LENGTH AT PRE-LOAD (INSTALLED) IS 6.5mm.
4. RADIAL EXTENSION AT CLOSED END MAY BE LOCATED AS SHOWN OR ROTATED 180ø.
5. TORQUE AT PRE-LOAD: $3.5X10^{-3}$ Nm $\pm 0.5X10^{-3}$ Nm.
6. [6] FULL LOAD CONDITION: BASIC SHAPE OF SPRING SHALL BE CONICAL SUCH THAT INDIVIDUAL WINDINGS WILL NOT BIND AGAINST ADJACENT WINDINGS WHEN COIL IS COMPRESSED TO 1.5MM AND TORQUED CCW 70° FROM PRE-LOAD CONDITION.
7. AXIAL LOAD AT PRE-LOAD: 0.25 ±0.05 NEWTONS.
8. SPRING SHOWN IN FREE STATE.

FIGURE 6-45. SPRING, LATCH

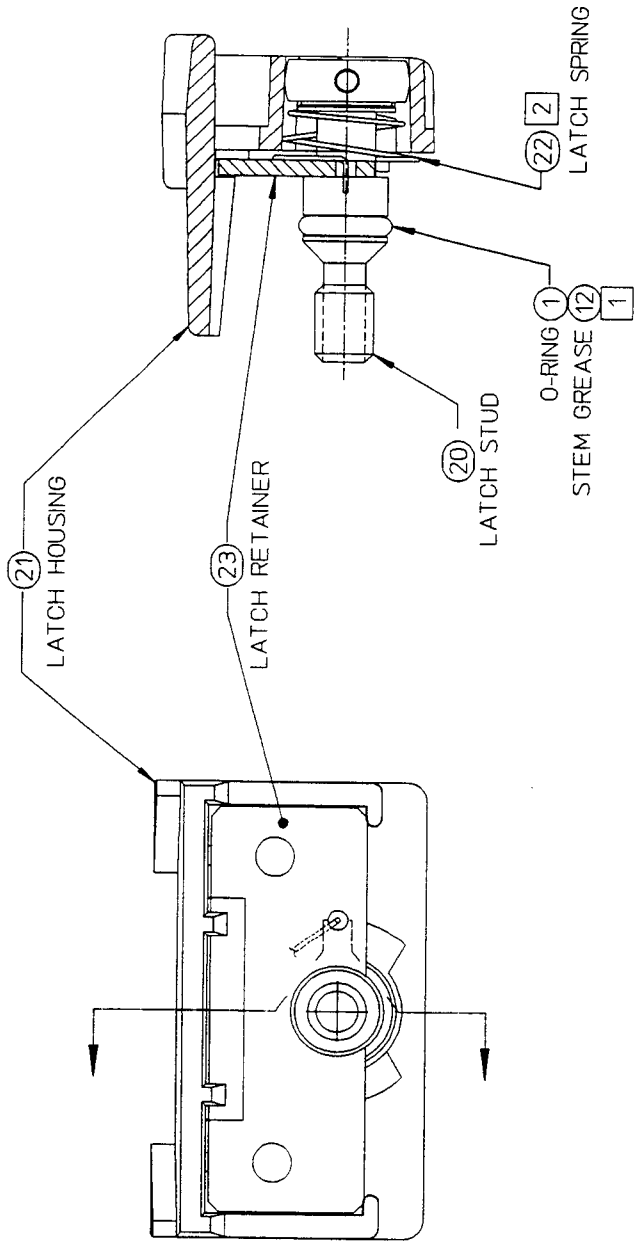


NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: STAINLESS STEEL SHEET 1.57mm THICK, AISI304 / UNS S30400.

2. FINISH: PASSIVATE PER QQ-P-35.

FIGURE 6-46. RETAINER, LATCH

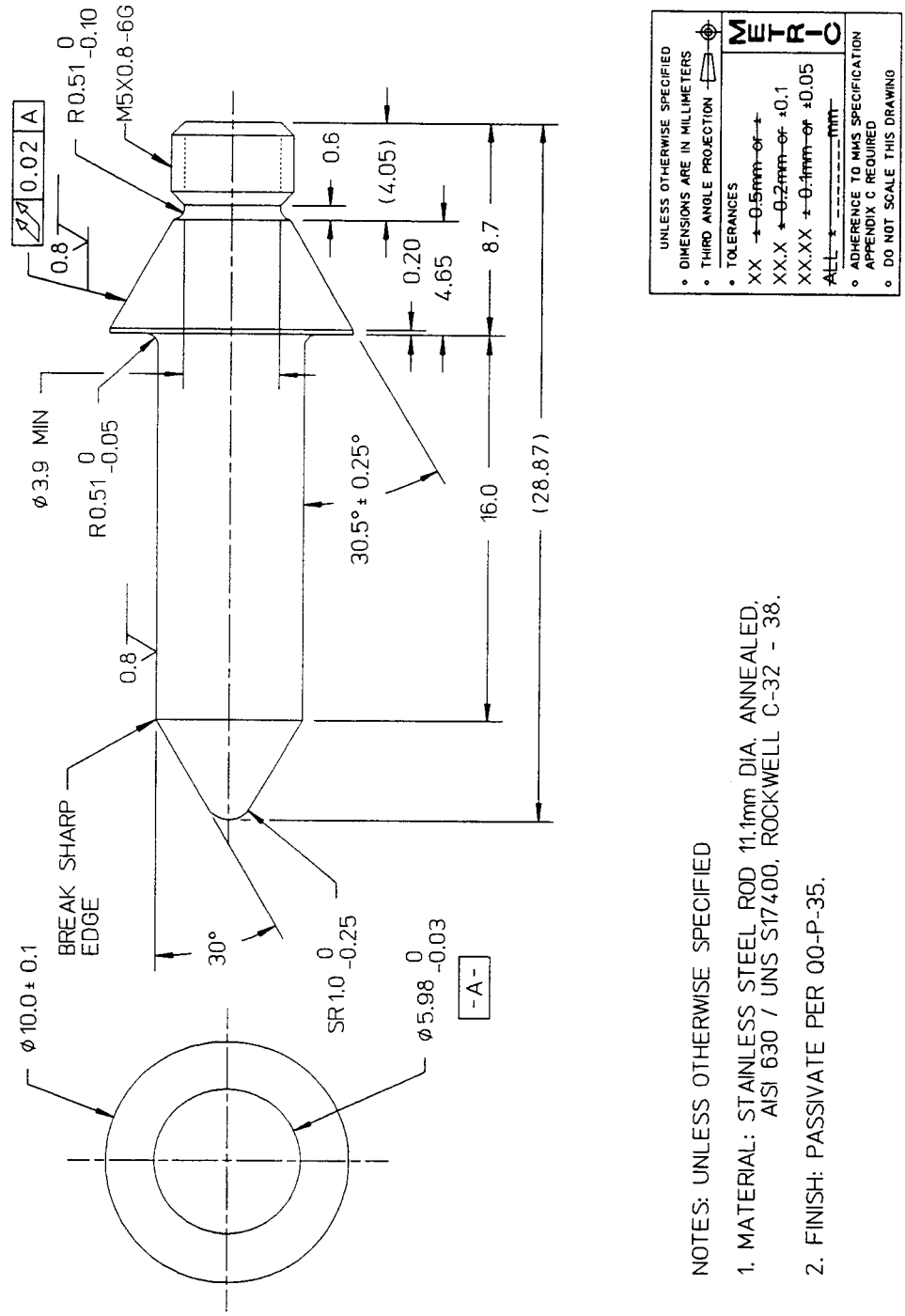


NOTES: UNLESS OTHERWISE SPECIFIED

[1] RECOMMENDATION LIGHTLY COAT O-RING (ITEM 1) WITH STEM GREASE (ITEM 12) BEFORE INSTALLING O-RING ONTO LATCH STUD (ITEM 20).

[2] INSTALL SMALL END DIAMETER TANG OF LATCH SPRING (ITEM 22) INTO THE ø0.8 HOLE OF THE LATCH STUD (ITEM 20 SEE FIG.6-43). INSTALL LARGE END DIAMETER TANG INTO THE ø2.0 HOLE OF THE RETAINER (ITEM 23 SEE FIG.6-46). PLACE THIS SUB-ASSEMBLY INTO THE LATCH HOUSING (ITEM 21) AS SHOWN.

FIGURE 6-47. MAINFRAME LATCH ASSEMBLY

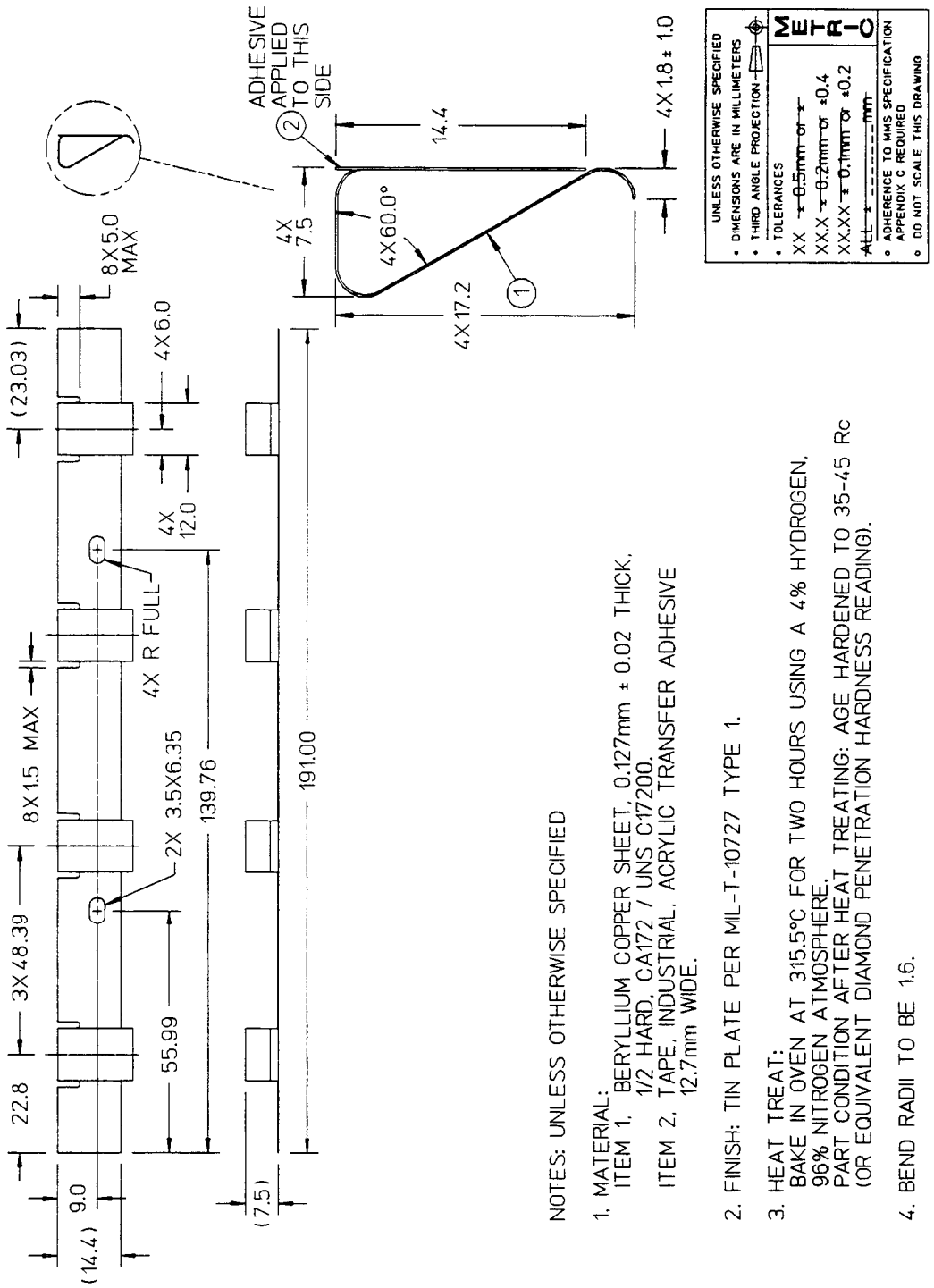


NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: STAINLESS STEEL ROD 11.1mm DIA. ANNEALED, AISI 630 / UNS S17400, ROCKWELL C-32 - 38.

2. FINISH: PASSIVATE PER QQ-P-35.

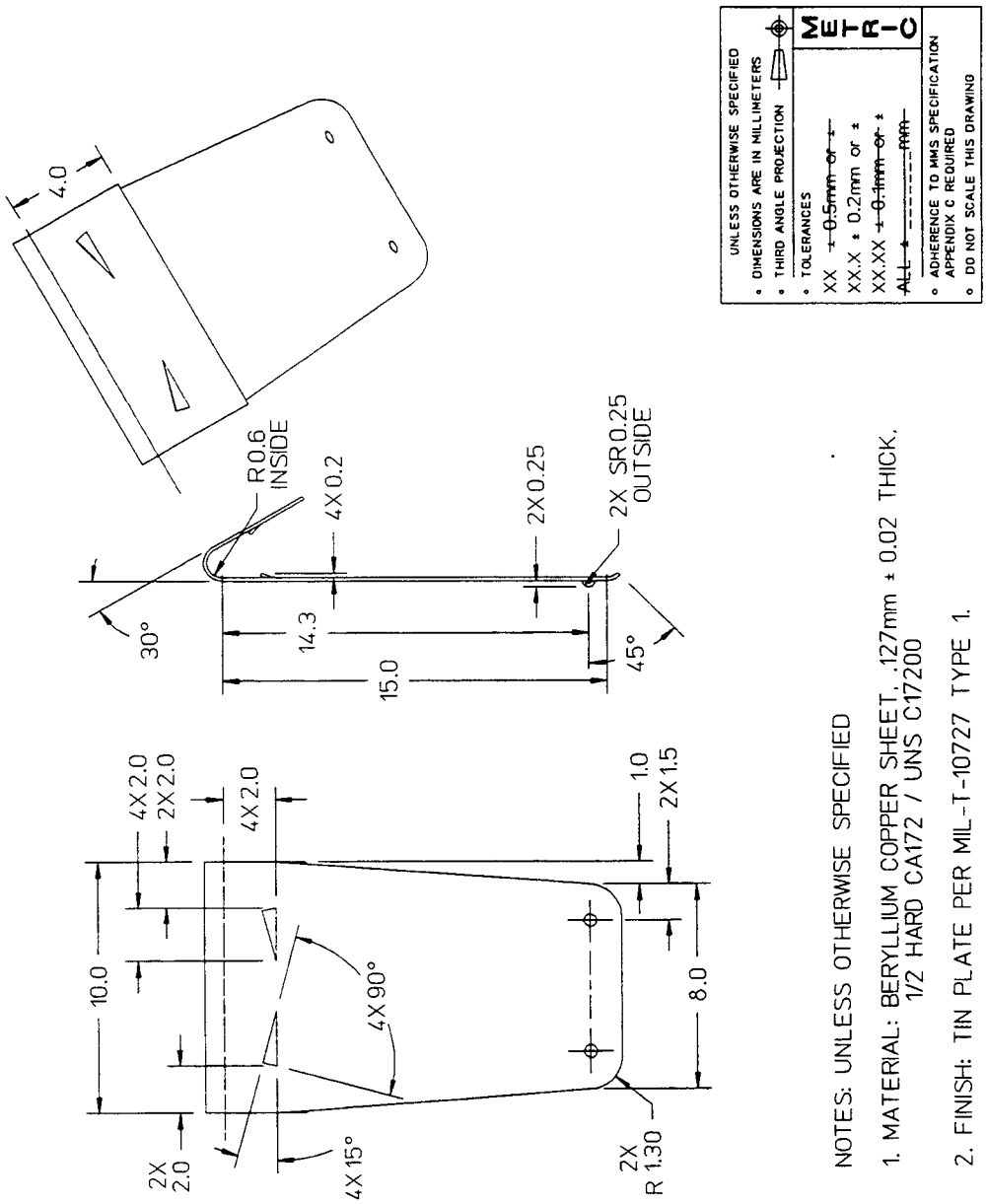
FIGURE 6-48. PIN, MAINFRAME GUIDE



NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL:
   ITEM 1. BERYLLIUM COPPER SHEET, 0.127mm ± 0.02 THICK, 1/2 HARD, CA172 / UNS C17200.
   ITEM 2. TAPE, INDUSTRIAL, ACRYLIC TRANSFER ADHESIVE 12.7mm WIDE.
2. FINISH: TIN PLATE PER MIL-T-10727 TYPE 1.
3. HEAT TREAT:
   BAKE IN OVEN AT 315.5°C FOR TWO HOURS USING A 4% HYDROGEN, 96% NITROGEN ATMOSPHERE.
   PART CONDITION AFTER HEAT TREATING: AGE HARDENED TO 35-45 Rc (OR EQUIVALENT DIAMOND PENETRATION HARDNESS READING).
4. BEND RADII TO BE 1.6.

FIGURE 6-49. SPRING, GROUND, TOP FRONT



NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: BERYLLIUM COPPER SHEET, .127mm ± 0.02 THICK, 1/2 HARD CA172 / UNS C17200

2. FINISH: TIN PLATE PER MIL-T-10727 TYPE 1.

FIGURE 6-50. SPRING, GROUND, TOP REAR

NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: ITEM 1, BERYLLIUM COPPER SHEET, .127 mm ± 0.02 THICK,1/2 HARD, CA172 / UNS C17200.
   ITEM 2, TAPE, INDUSTRIAL, ACRYLIC TRANSFER ADHESIVE 12.7 mm WIDE.

2. FINISH: TIN PLATE PER MIL-T-10727 TYPE 1.

3. HEAT TREAT: BAKE IN OVEN AT 315.5°C FOR TWO HOURS USING A 4% HYDROGEN, 96% NITROGEN ATMOSPHERE.
   PART CONDITION AFTER HEAT TREATING: AGE HARDENED TO 35-45 Rc (OR EQUIVALENT DIAMOND PENETRATION HARDNESS READING).

[4] FREE END OF SPRING MAY NOT BE IN CONTACT WITH FLAT SURFACE ABOVE DATUM "A". DUE TO WARPING AFTER HEAT TREATMENT.MAXIMUM HEIGHT OF UNRESTRAINED FREE END OF SPRING ABOVE FLAT SURFACE IS 2.0. MEASURE 4.75 DIMENSION WITH FREE END CONTACTING DATUM "A" SURFACE.

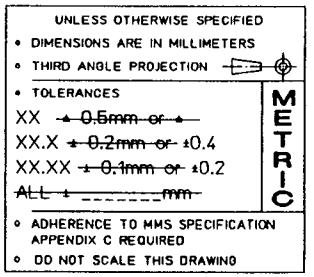


FIGURE 6-51. SPRING, GROUND, BOTTOM REAR SHEET 1 OF 2

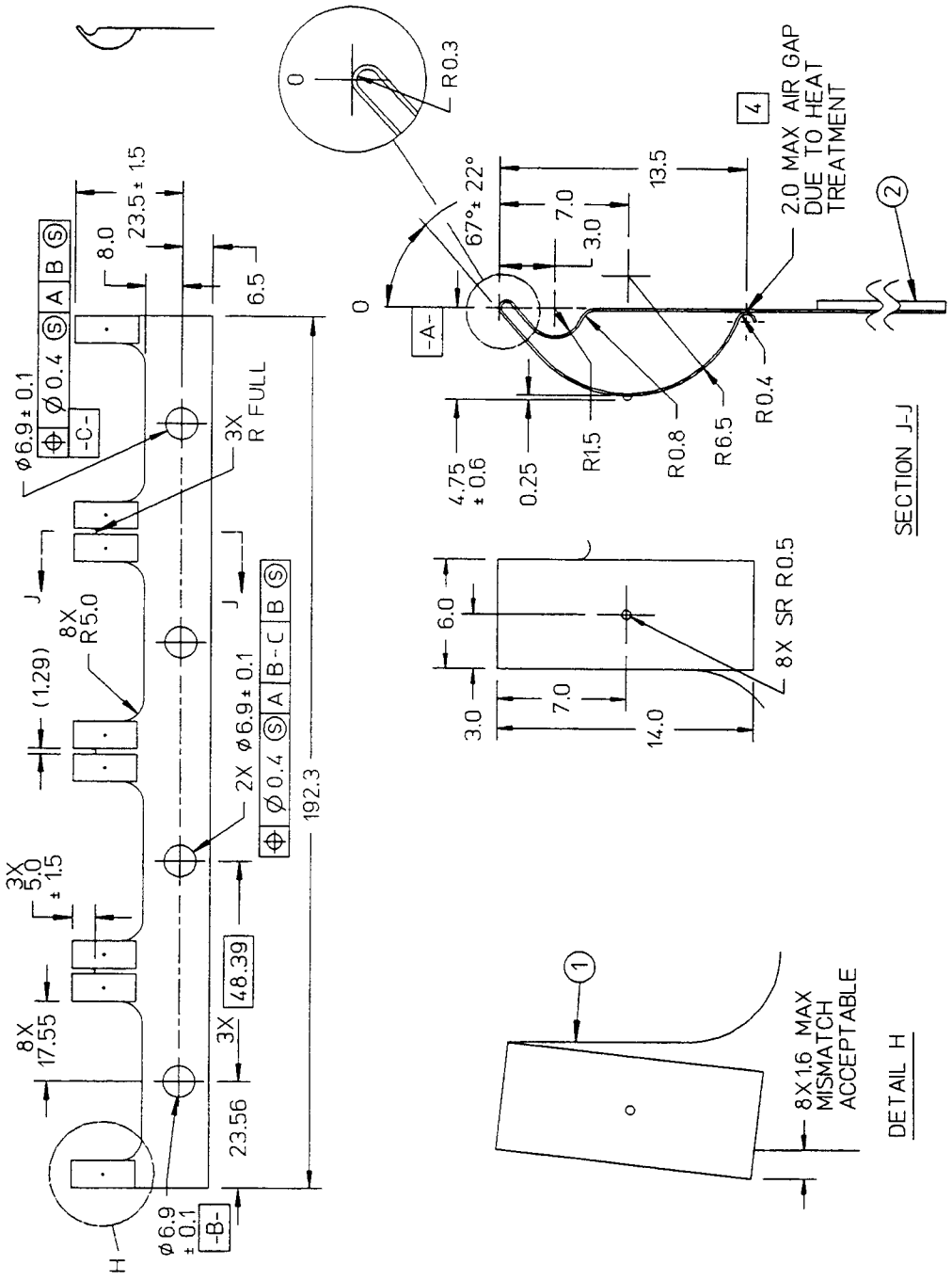


FIGURE 6-51. SPRING, GROUND, BOTTOM REAR SHEET 2 OF 2

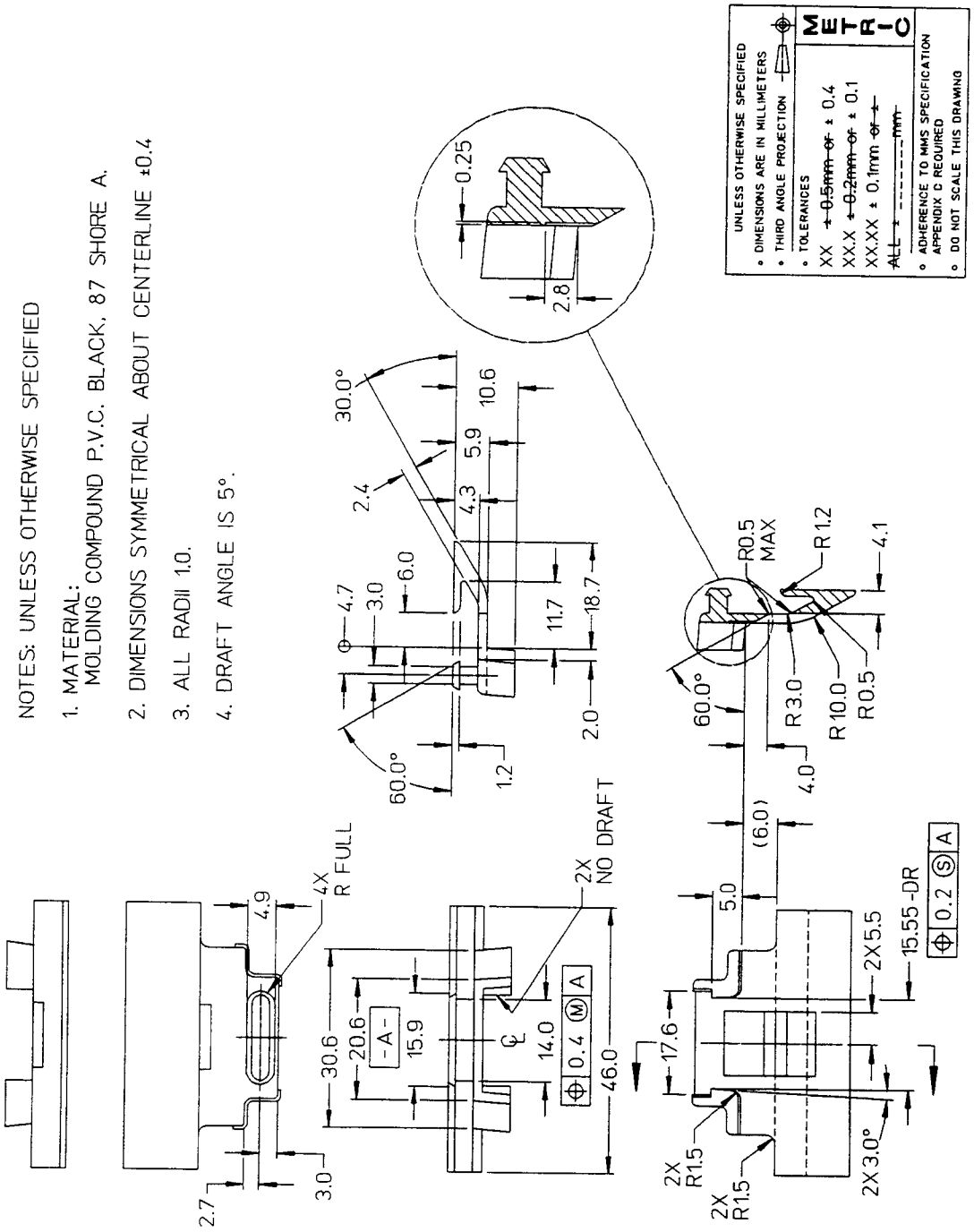


FIGURE 6-52. VIBRATION STOP

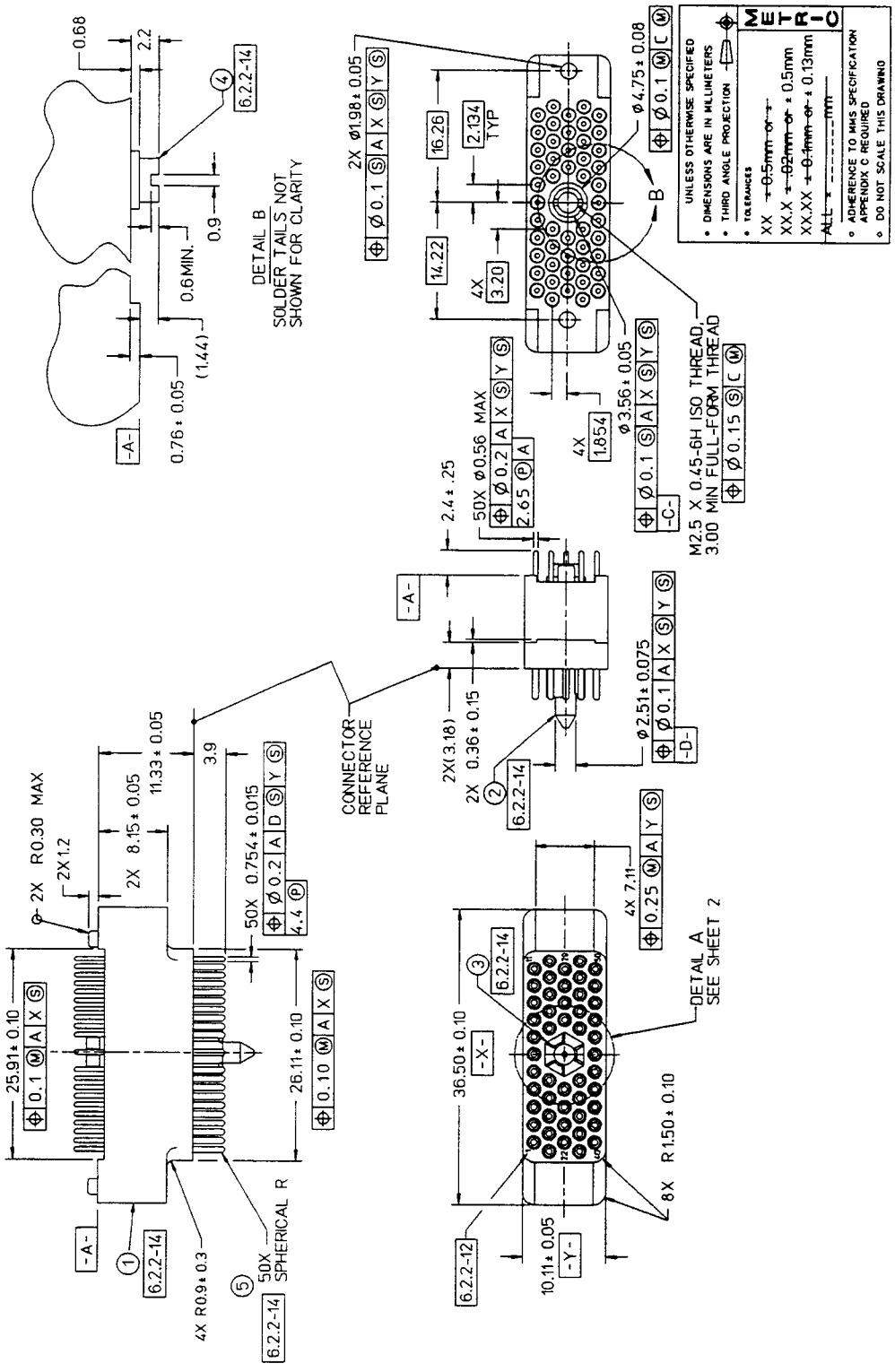
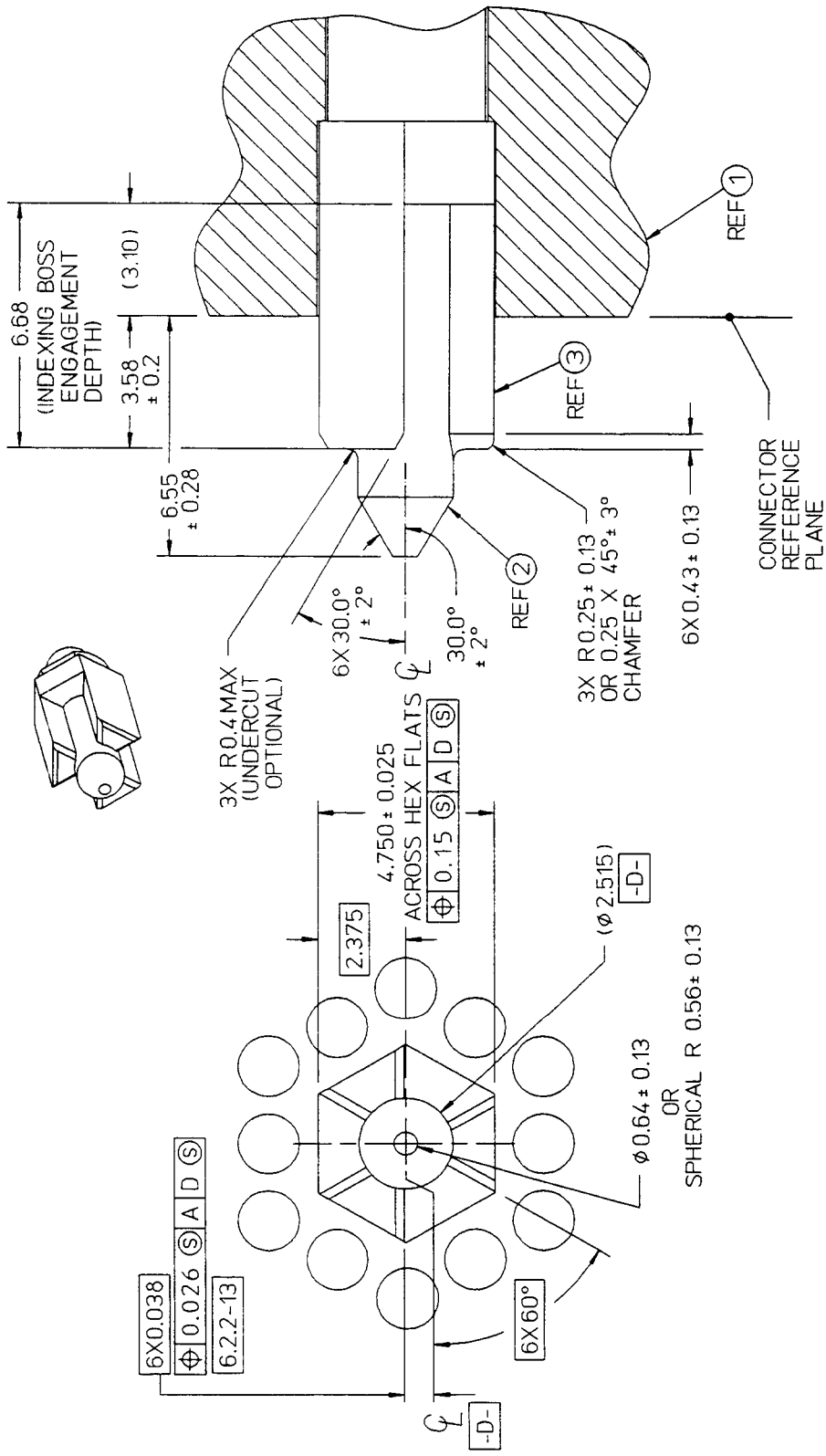


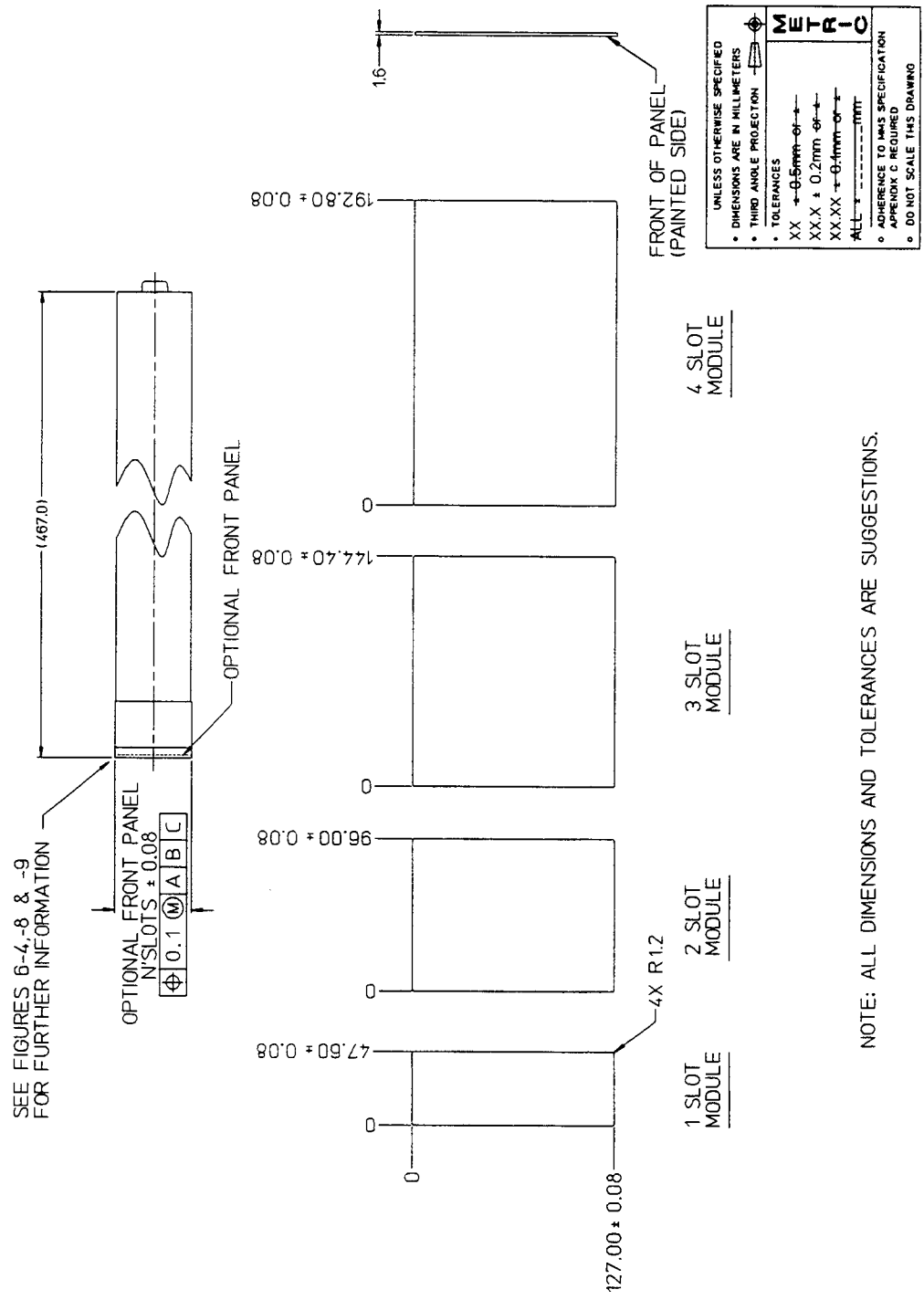
FIGURE 6-53. CONNECTOR,MAINFRAME MSIB SHEET 1 OF 2



DETAIL A

INDEXING BOSS DETAIL
SHOWN WITHOUT CONTACTS FOR CLARITY

FIGURE 6-53. CONNECTOR,MAINFRAME MSIB SHEET 2 OF 2



NOTE: ALL DIMENSIONS AND TOLERANCES ARE SUGGESTIONS.

FIGURE 6-56. MODULE OPTIONAL FRONT PANEL SIZES

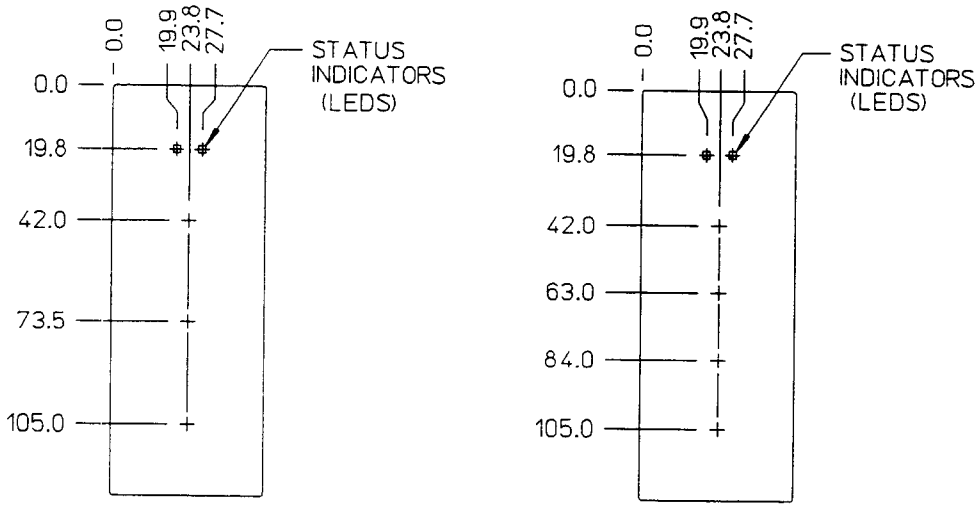
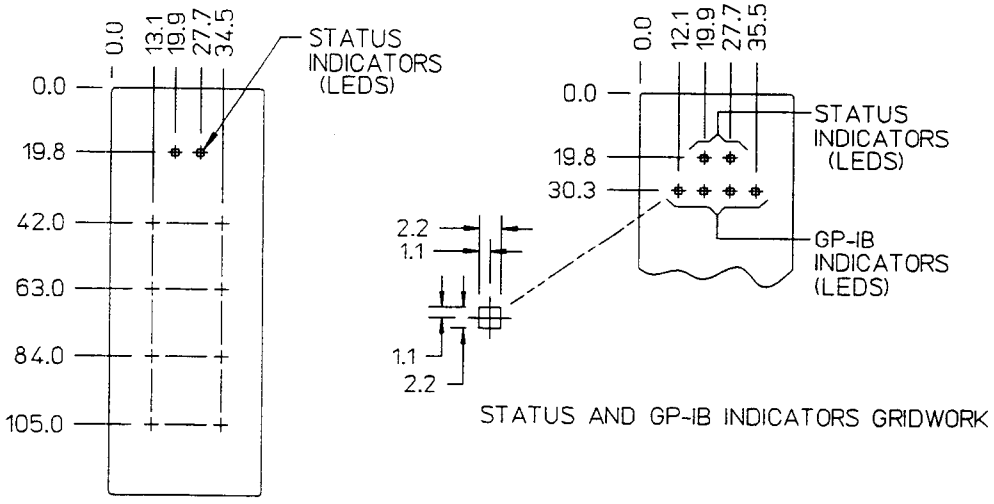


FIGURE 6-57. MODULE FRONT 3 & 4 COMPONENT GRIDWORK, 1 SLOT MODULE



STATUS AND GP-IB INDICATORS GRIDWORK

FIGURE 6-58. MODULE FRONT 8 COMPONENT GRIDWORK, 1 SLOT MODULE

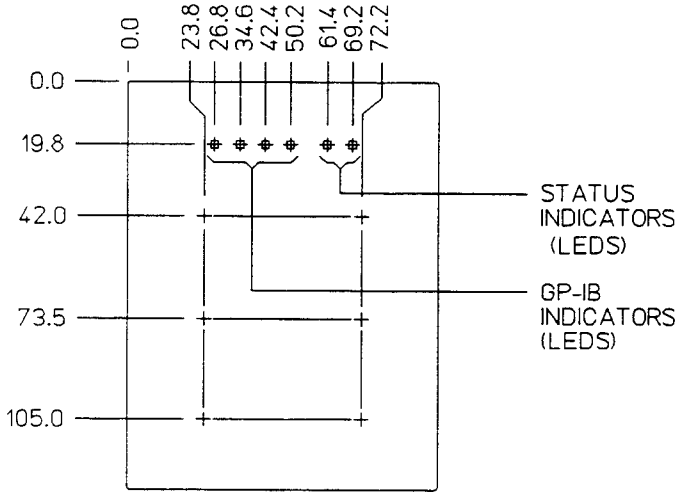


FIGURE 6-59. MODULE FRONT 6 COMPONENT GRIDWORK, 2 SLOT MODULE

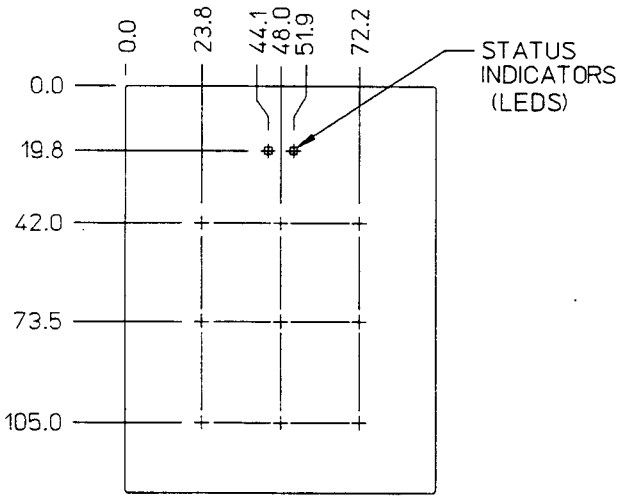


FIGURE 6-60. MODULE FRONT 9 COMPONENT GRIDWORK, 2 SLOT MODULE

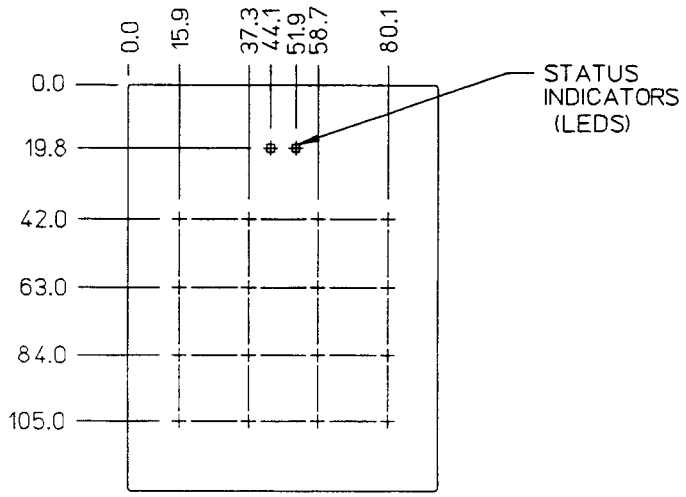


FIGURE 6-61. MODULE FRONT 16 COMPONENT GRIDWORK, 2 SLOT MODULE

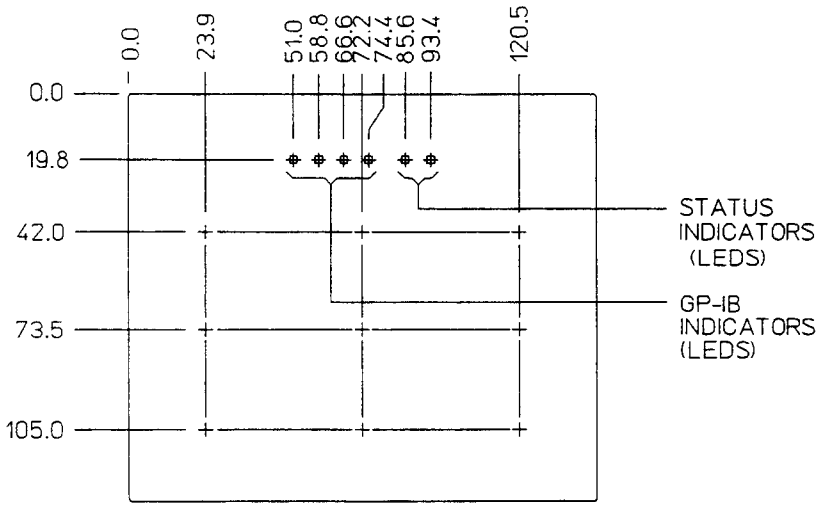


FIGURE 6-62. MODULE FRONT 9 COMPONENT GRIDWORK, 3 SLOT MODULE

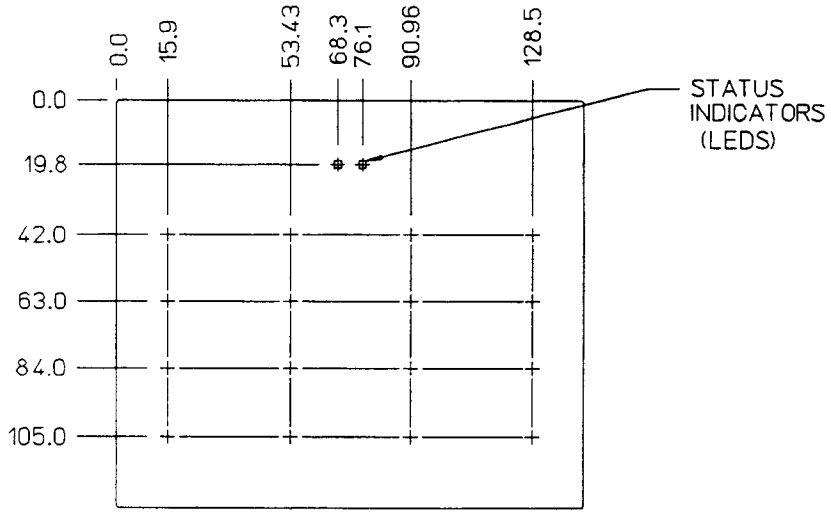


FIGURE 6-63. MODULE FRONT 16 COMPONENT GRIDWORK, 3 SLOT MODULE

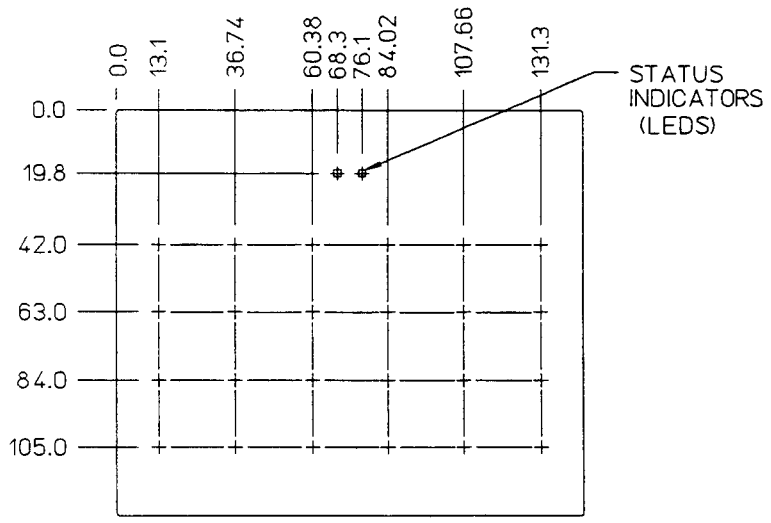


FIGURE 6-64. MODULE FRONT 24 COMPONENT GRIDWORK, 3 SLOT MODULE

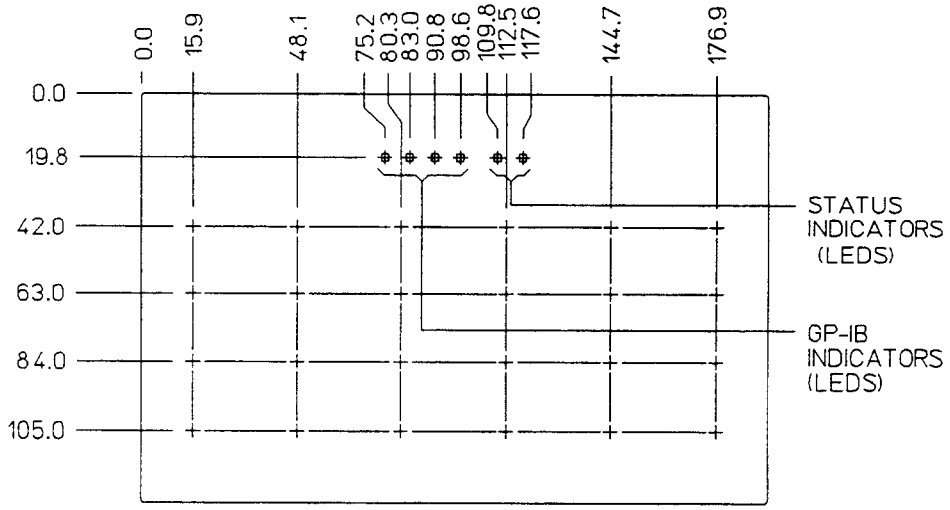


FIGURE 6-65. MODULE FRONT 24 COMPONENT GRIDWORK, 4 SLOT MODULE

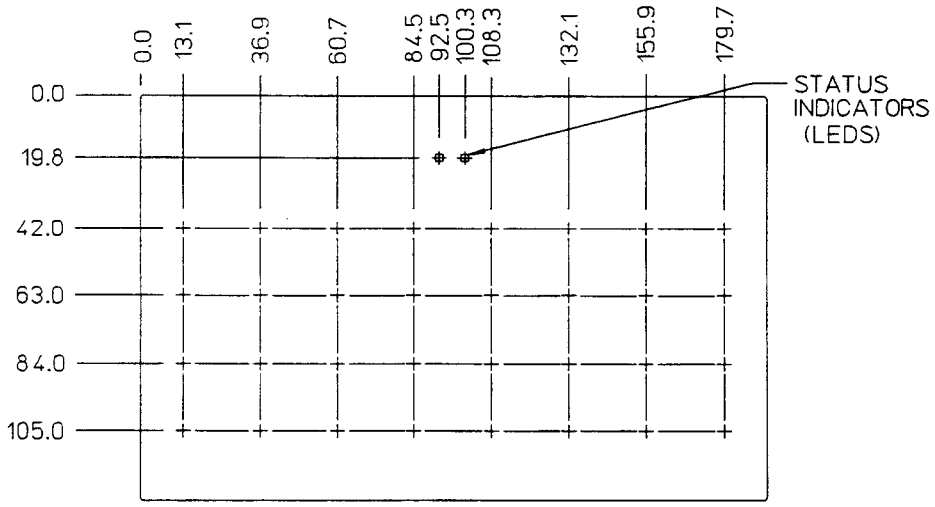
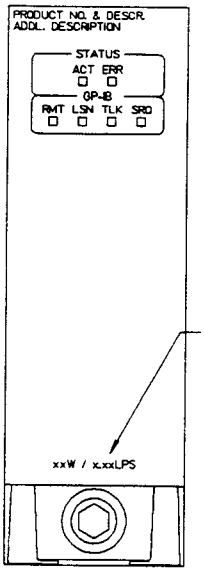


FIGURE 6-66. MODULE FRONT 32 COMPONENT GRIDWORK, 4 SLOT MODULE

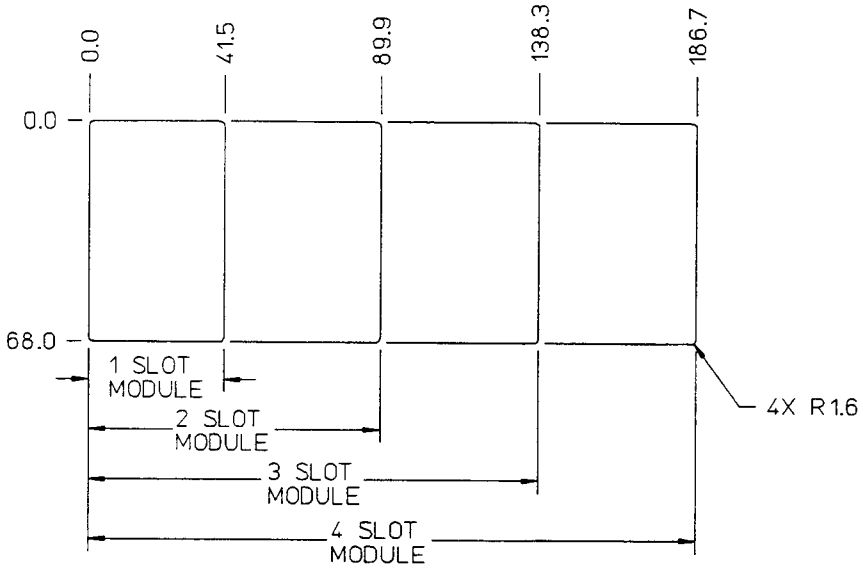


INDICATOR APPLICATION	LED COLOR
ERR (ERROR,STATUS) SELF TEST	RED
RMT (REMOTE,GP-IB) LSN (LISTEN,GP-IB) TLK (TALK,GP-IB) SRQ (SERVICE REQUEST,GP-IB)	YELLOW
ACT (ACTIVE,STATUS) MEASURE	GREEN

INDICATOR COLOR PARAMETERS

RED: CAUTION/WARNING APPLICATIONS
YELLOW: GENERAL/NORMAL APPLICATIONS
GREEN: ACTIVATED/ON APPLICATIONS

FIGURE 6-67. MODULE FRONT INDICATORS AND NOMENCLATURE



NOTE:
1. ALL DIMENSIONS AND TOLERANCES ARE SUGGESTIONS.
2. THESE PANEL SIZES APPLY TO BOTH LABELS AND REMOVABLE PANELS.

FIGURE 6-68. MODULE OPTIONAL REAR PANEL SIZES

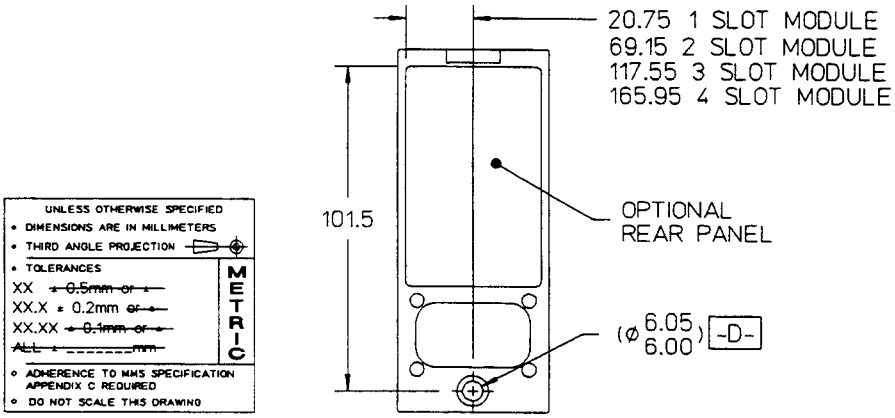


FIGURE 6-69. MODULE REAR DATUM REFERENCES

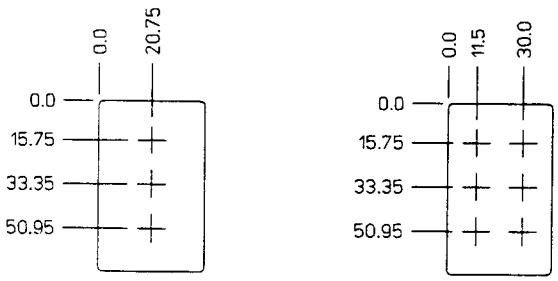


FIGURE 6-70. MODULE REAR 3 & 6 COMPONENT GRIDWORK, 1 SLOT MODULE

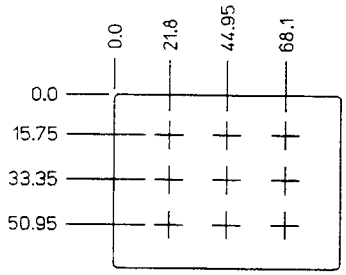


FIGURE 6-71. MODULE REAR 9 COMPONENT GRIDWORK, 2 SLOT MODULE

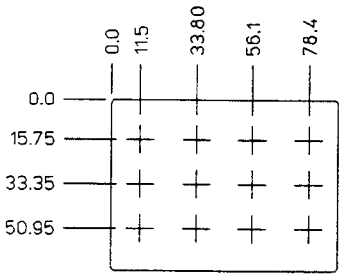


FIGURE 6-72. MODULE REAR 12 COMPONENT GRIDWORK, 2 SLOT MODULE

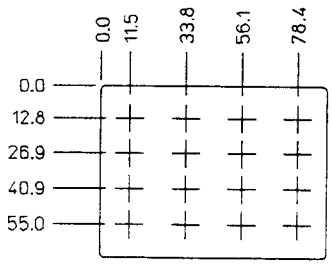


FIGURE 6-73. MODULE REAR 16 COMPONENT GRIDWORK, 2 SLOT MODULE

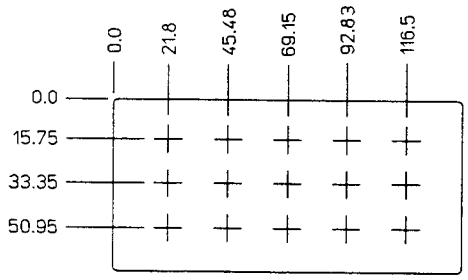


FIGURE 6-74. MODULE REAR 15 COMPONENT GRIDWORK, 3 SLOT MODULE

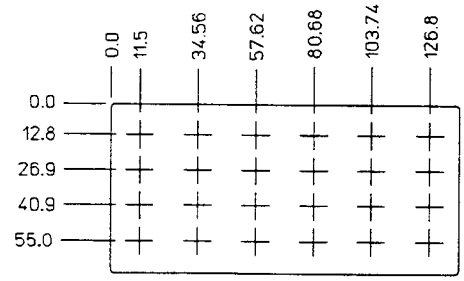


FIGURE 6-75. MODULE REAR 24 COMPONENT GRIDWORK, 3 SLOT MODULE

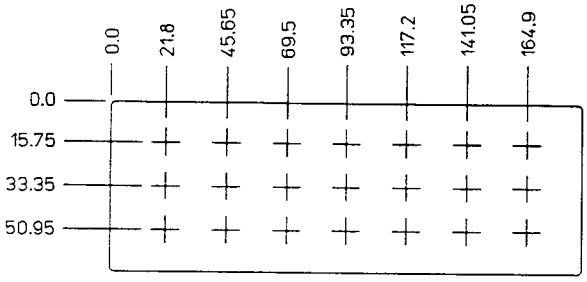


FIGURE 6-76. MODULE REAR 21 COMPONENT GRIDWORK, 4 SLOT MODULE

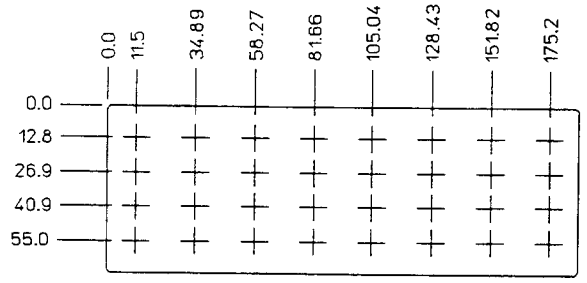


FIGURE 6-77. MODULE REAR 32 COMPONENT GRIDWORK, 4 SLOT MODULE

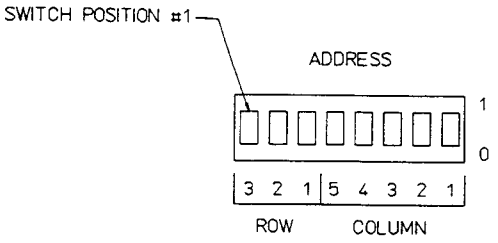


FIGURE 6-78. MODULE SYSTEM ADDRESS GRAPHICS

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7. COOLING SPECIFICATIONS

7.1 Mainframe Cooling

RULE 7.1-1:
Cooling air **MUST** flow from an MMS mainframe into an MMS module as shown in figure 7-1.

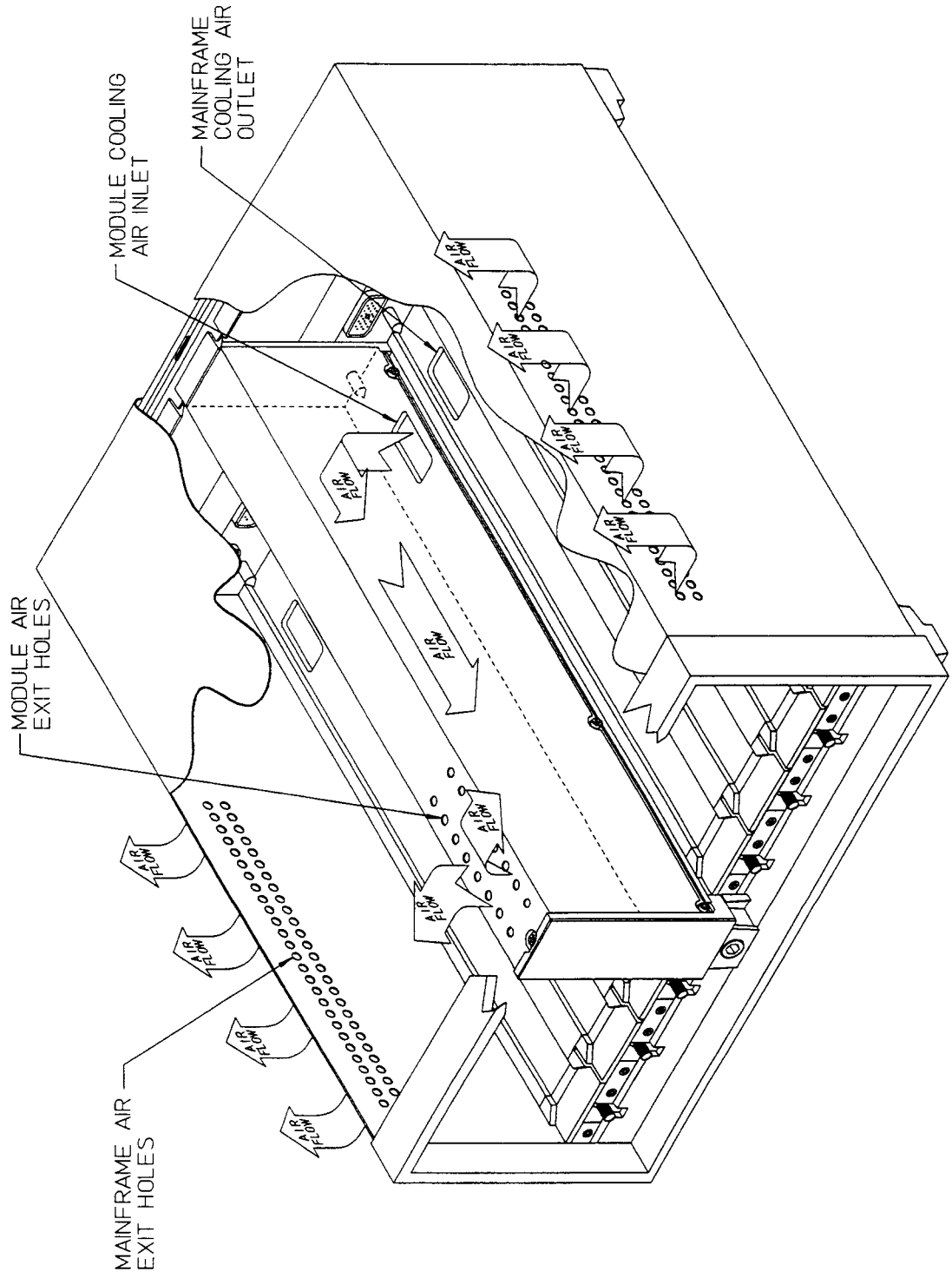

Figure 7-1. Mainframe Cooling Overview

RULE 7.1-2:

The minimum specified airflow supplied per module slot **MUST** be established by measuring worst case minimum airflow though a module whose resistance characteristics are equal to, or slightly greater than, the formula below. See figure 7-2 for a graphical representation, and appendix B.5.1 for testing information.

$$\Delta P = 0.62 \times (Q)^2 \text{ (Based on Standard Air)}$$

where,

ΔP = Static pressure drop across module (mm H2O),
Q = Airflow volume (Liters per second)

OBSERVATION 7.1-3:

"Worst case minimum airflow" is typically found by identifying the slot with the lowest airflow and testing it with all other slots empty.

OBSERVATION 7.1-4:

The resistance characteristic of the mainframe airflow measurement module, specified in rule 7.1-2, was selected as representative of worst case component packing density. It is unlikely that actual MMS modules will have resistance to airflow equal to or greater than this module.

RULE 7.1-5:

A decrease in airflow due to a resistance characteristic greater than specified in rule 7.1-2 **MUST** be established in an MMS mainframe. This decrease shall be established by measuring worst case minimum airflow though a module whose resistance characteristics are equal to, or slightly greater than, the formula below. The decrease in airflow caused by the larger resistance **MUST NOT** be greater than 35% of that found in rule 7.1-2. See figure 7-2 and appendix B.5.1.

$$\Delta P = 0.90 \times (Q)^2 \text{ (Based on Standard Air)}$$

where,

ΔP = Static pressure drop across module (mm H2O),
Q = Airflow volume (Liters per second)

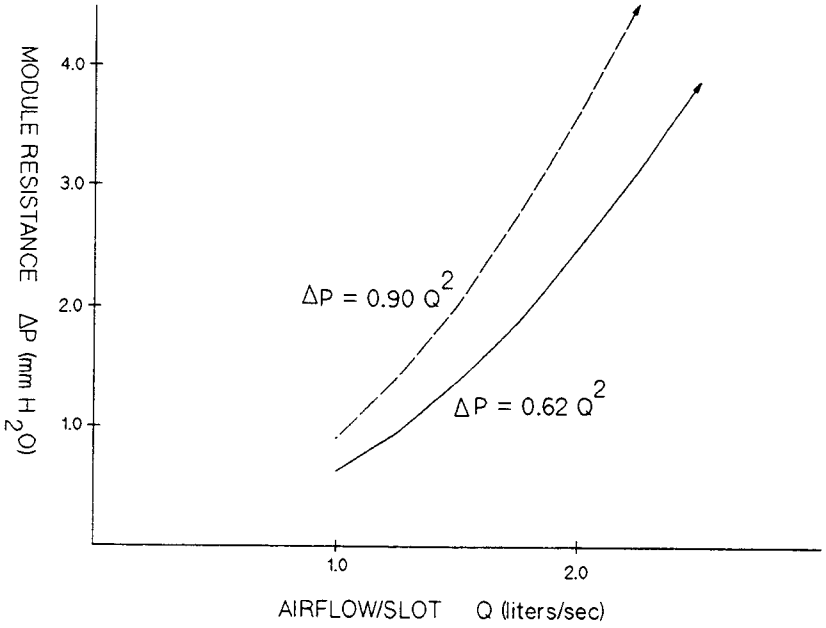

Figure 7-2. Module Resistance Curves

OBSERVATION 7.1-6:

Specifying the maximum decrease in airflow with an unusually high pressure drop module forces mainframe designers to select fans and fan operating points which guarantee stable operation under all conceivable conditions.

PERMISSION 7.1-7:

For acoustic purposes, a reduction in airflow from the minimum specified airflow is allowed below an ambient temperature of 50 degrees Celsius.

RULE 7.1-8:

Airflow reductions allowed in permission 7.1-7 **MUST** keep the bulk temperature under the limits specified in figure 7-3. The bulk temperature calculations for comparison with figure 7-3 **MUST** start with a 15 degree Celsius average air temperature rise based on the minimum specified airflow at an ambient temperature of 50 degree Celsius. The increased average air temperatures below an ambient of 50 degrees Celsius, due the the airflow reductions, **MUST** be calculated assuming a constant power dissipation.

OBSERVATION 7.1-9:

Bulk temperature, for the purposes of the MMS specification, is defined as the ambient air temperature plus the average air temperature rise through a module.

OBSERVATION 7.1-10:

Rule 7.1-8, see figure 7-3, defines the worst case bulk temperature characteristic that MMS module designers may face when MMS mainframe designs limit airflow for acoustic purposes. For comparison, figure 7-4 shows the effect of this limit on other temperature rise designs. Note that a module designed for a temperature rise in excess of 15 degrees Celsius can experience a maximum bulk temperature when ambient is below 50 degrees. Having bulk temperature calculations based on a

15 degree Celsius average air temperature rise is a trade off between MMS mainframe and MMS module designs. A higher average air temperature rise for the curve shown in figure 7-3, e.g., 20 degrees Celsius, would limit the ability of MMS mainframe designs to reduce acoustic noise. Having a lower average air temperature rise for figure 7-3 would limit cooling options for MMS module design.

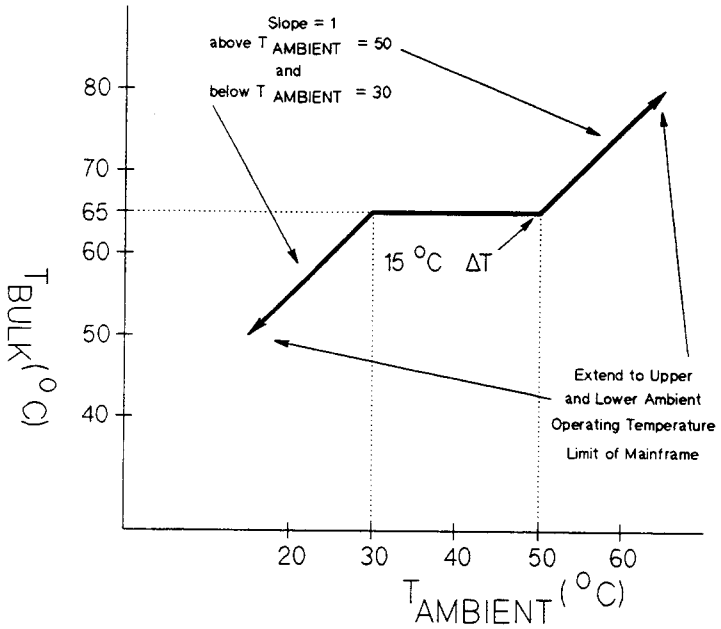

Figure 7-3. Airflow Reduction Bulk Temperature Limit (Use 15° C ΔT)

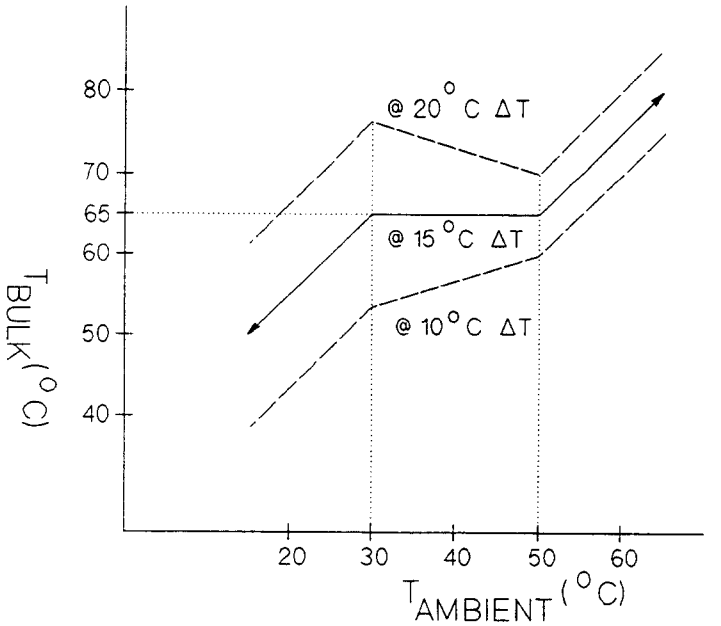

Figure 7-4. Temperature Rise Comparison

OBSERVATION 7.1-11:
A reduction in airflow below 30 degrees Celsius is usually not necessary. The ambient temperature range where acoustic performance is typically most important is 30 degrees Celsius and below.

SUGGESTION 7.1-12:
MMS mainframe designs should provide the maximum airflow possible at all ambient operating temperatures within the constraints of acoustic requirements.

RULE 7.1-13:
An MMS mainframe **MUST** deliver a minimum of 1.00 liter per second per module slot under all operating conditions.

OBSERVATION 7.1-14:
Rule 7.1-13 specifies that at least 1.00 liter per second of airflow be supplied regardless of ambient conditions. This is an additional constraint to the airflow reduction limits as called out by rule 7.1-8. In other words, airflow can be reduced from its minimum specified airflow for acoustic reasons as long as it meets the bulk temperature requirements shown in figure 7-3 and never falls below 1.00 liter per second.

RULE 7.1-15:
An MMS mainframe **MUST NOT** raise the temperature of air entering modules more than 5 degrees Celsius above ambient under all operating conditions.

OBSERVATION 7.1-16:
The allowable average air temperature rise called out in rule 7.1-15, up to 5 degrees Celsius, is always assumed to be zero when calculating bulk temperature for the purposes of mainframe airflow reduction as called out in rule 7.1-8. In actual operation, the module exit air temperature of a module with a 15 degree Celsius average air temperature rise could be as much as 5 degree Celsius higher than that shown as T-BULK in figure 7-3.

OBSERVATION 7.1-17:
MMS mainframes are required to list on a capability label their minimum specified airflow per slot, in liters per second. See chapter 9, *Capability Labeling.*

OBSERVATION 7.1-18:
When configuring an MMS mainframe without a capability label, 1.25 liters per second can be assumed when no other information is available. It is best to consult the manufacturer of an unlabeled MMS mainframe to determine its specified airflow.

SUGGESTION 7.1-19:
MMS mainframes should be designed to provide at least 1.25 liters per second of airflow. A large installed base of MMS modules exist with this minimum required airflow.

7.2 Module Cooling

RULE 7.2-1:
Minimum cooling requirements, in liters per second per module slot, **MUST** be determined for a module.

OBSERVATION 7.2-2:
Minimum cooling requirements are specified on a per slot basis for both MMS modules and MMS mainframes. This allows a systems integrator to check only a single value between mainframes and modules to decide if sufficient airflow is supplied.

OBSERVATION 7.2-3:
The minimum required airflow for an MMS module is based upon the manufacturers reliability goals. These goals take into account the environmental conditions that are specified for the product.

RULE 7.2-4:
Specified minimum cooling requirements for an MMS module **MUST** take into account the allowable mainframe fan speed reduction limits, as called out in rule 7.1-8. See figure 7-3.

RULE 7.2-5:
Specified minimum cooling requirements for an MMS module **MUST** take into account the allowable ambient temperature rise before air enters a module called out in rule 7.1-15.

RECOMMENDATION 7.2-6:
MMS modules should be tested to determine the pressure drop characteristic at the minimum required airflow. See appendix B.5.2 for testing information.

OBSERVATION 7.2-7:
Mainframes are required to supply a minimum airflow of 1.00 liter per second under all operating conditions.

OBSERVATION 7.2-8:
MMS modules are required to list on a capability label the required airflow per slot, in liters per second. See chapter 9, *Capability Labeling*.

OBSERVATION 7.2-9:
When configuring an MMS mainframe with MMS modules that lack capability labeling, 1.25 liters per second can be assumed when no other information is available. It is best to consult the manufacturer of an unlabeled MMS module to determine its minimum required airflow.

OBSERVATION 7.2-10:
MMS module airflow requirements, when possible, should be limited to 1.25 liters per second. A large installed base of MMS mainframes exist that meet this minimum specified airflow.

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8. ELECTROMAGNETIC COMPATIBILITY (EMC)

8.1 Module Electromagnetic Compatibility

The following requirements apply to modules. The intent of these requirements is to assure electromagnetic compatibility between modules and between modules and mainframes. To that end, the focus of this specification is on the interfaces between modules and mainframes. Radiated emissions and susceptibility at the surface of modules are specified. Conducted emissions and susceptibility on the 40 kHz power bus and the IEEE-488.1 and MSIB buses are specified.

These requirements do not address electromagnetic interaction between modules and the external environment. Radiated emissions and susceptibility beyond the confines of a mainframe are not specified. Conducted emissions and susceptibility onto the mainframe's power line are not specified.

RECOMMENDATION 8.1-1:

MMS module manufacturers should specify which regulatory or other EMC standards they comply with.

8.1.1 Module Radiated EMC

This specification does not dictate the particular set of regulatory EMC standards with which a module must comply. It does not require adherence to, for example, FCC, VDE, or Mil Spec EMC requirements.

8.1.1.1 Module Radiated Emissions

RECOMMENDATION 8.1.1.1-1:

If a module manufacturer specifies compliance to a given set of regulatory EMC standards, it is recommended that the modules be tested individually in a mainframe to the limits of the specification. It is not necessary to derate the specification limit based on module size. The purpose of this recommendation is to ensure that EMC claims by different manufacturers have a common definition. This will ease the burden on system integrators who wish to design a system meeting specific regulatory EMC requirements.

OBSERVATION 8.1.1.1-2:

A system composed of multiple modules may have radiated emissions levels higher than that of the modules when tested individually. If a system is to meet a given radiated emissions specification, the radiated emissions levels of the individual modules may need to be lower.

8.1.1.1.1 Module Magnetic Field Radiated Emissions

RULE 8.1.1.1.1-1:

The close-field magnetic emissions measured on the surfaces of the module **MUST NOT** exceed the limit shown in figure 8-1. Emissions are specified at the left and right sides of the module. Emissions are not specified at the top, bottom, front, or rear of the module. The probe used to measure the magnetic field emissions **MUST** have an aperture of less than 100 mm^2. The suggested test procedure for this requirement is described in section B.2.1.

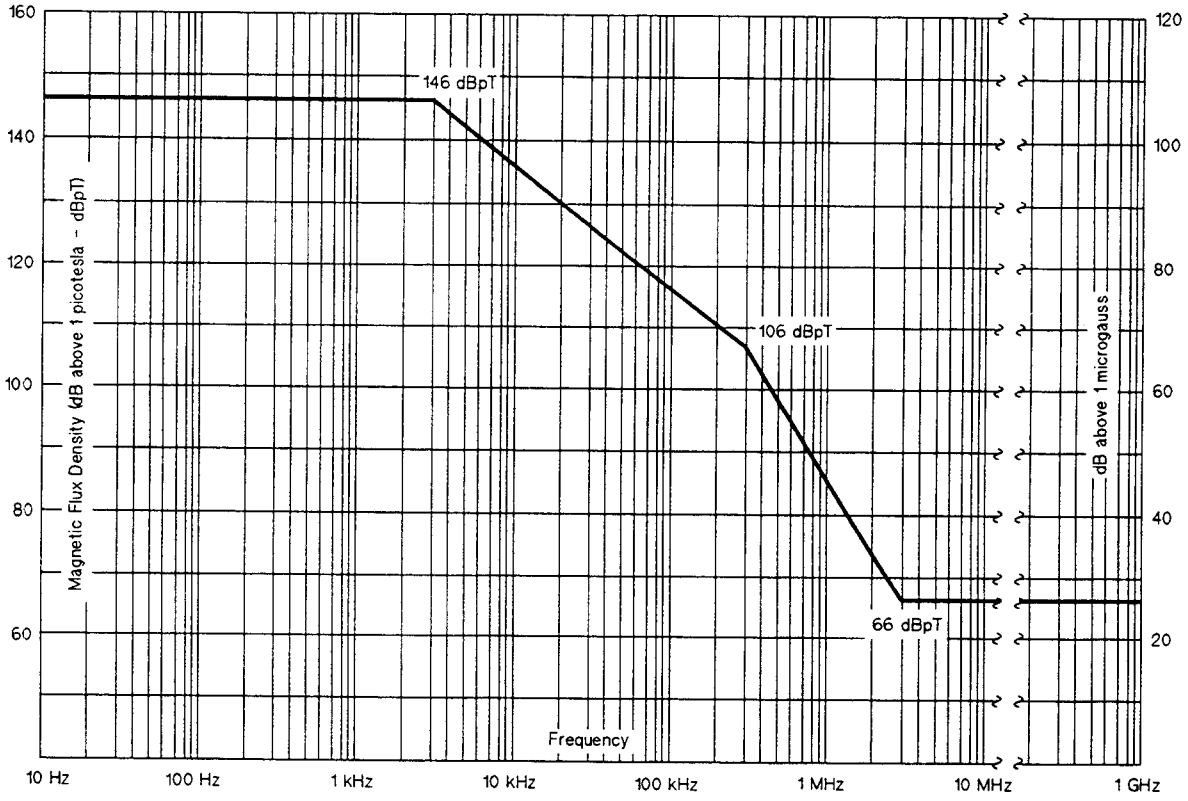

Figure 8-1. Close-field Magnetic Emission Limits

SUGGESTION 8.1.1.1.1-2:

In order to reduce the level of radiation of MSIB related signals from module surfaces, a ferrite core should be placed around all MSIB and IEEE-488.1 lines as a common mode choke, as shown in figure 8-2. The purpose of this choke is to force MSIB related return currents to flow through the backplane interface connector wiring rather than along the outside surface of the module. For this choke to work properly, MSIB and IEEE-488.1 returns need to be routed through the core along with the signal lines. The 40 kHz power lines and return should not be routed through this core, as this will induce 40 kHz power supply voltages onto the buses.

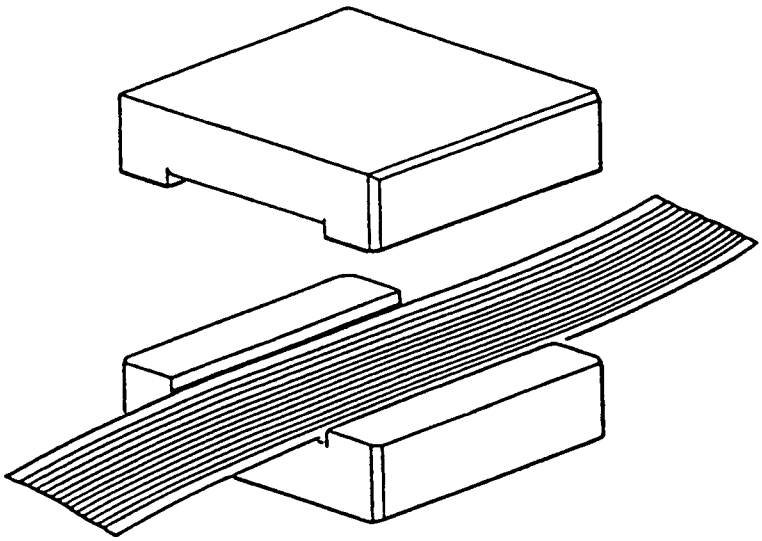

Figure 8-2. Flex Circuit and Ferrite - exploded view

8.1.1.1.2 Module Electric Field Radiated Emissions

Near field electric field emissions are not specified. The accuracy of electric field measurements near metal surfaces is poor, and magnetic fields are a more severe threat.

8.1.1.2 Module Radiated Susceptibility

In order to assure compatibility between modules and between modules and mainframes, near field magnetic susceptibility is specified for the module.

8.1.1.2.1 Module Magnetic Field Susceptibility

RULE 8.1.1.2.1-1:

The close field magnetic susceptibility measured on the surfaces of the module **MUST** be below the limit shown in figure 8-3. Susceptibility is specified at the left and right sides of the module. Susceptibility is not specified at the top, bottom, front, or rear of the module. The probe used to generate the magnetic field for this test **MUST** have an aperture of greater than 25 mm^2. The suggested test procedure for this requirement is described in section B.2.2.

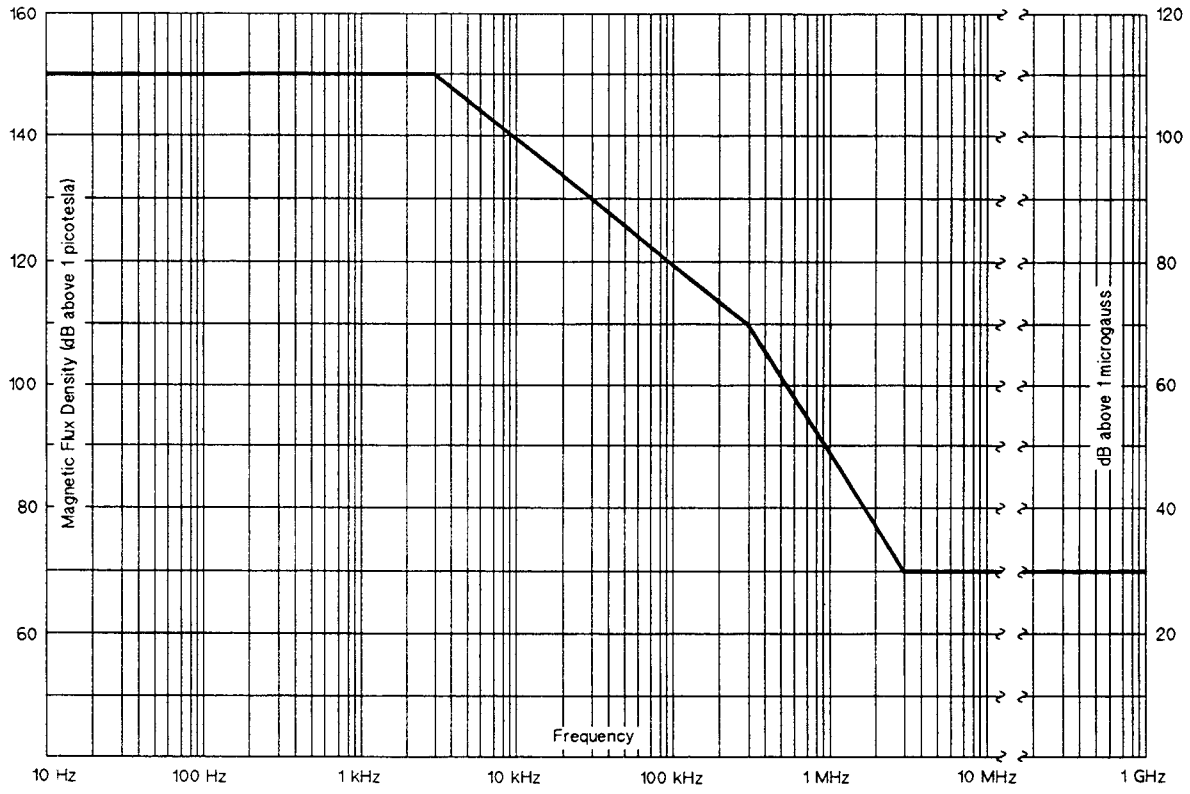

Figure 8-3. Close-field Magnetic Susceptibility Limits

8.1.1.2.2 Module Electric Field Susceptibility

Near field electric field susceptibility is not specified. The accuracy of electric field measurements near metal surfaces is poor, and magnetic fields are a more severe threat in the module.

8.1.2 Module Conducted EMC

This specification does not dictate the particular set of regulatory EMC standards with which a module must comply. It does not require adherence to, for example, FCC, VDE, or Mil Spec EMC requirements.

In order to assure compatibility between modules and between modules and mainframes, conducted emissions are specified at the module to mainframe backplane interface connector.

8.1.2.1 Module Power Bus Conducted EMC

Modules receive power from a mainframe through their backplane interface connector. This power is delivered as a 40 kHz AC waveform wave, differentially balanced with respect to ground. In order to control interaction between modules and between modules and mainframes, module conducted emissions and susceptibility are specified.

8.1.2.1.1 Module Power Bus Conducted Emissions

The current a module draws from the 40 kHz power bus is nominally a 40 kHz square wave. Three aspects of this current are specified to control interaction between modules through the common impedance of the power supply bus. The maximum harmonic content of this waveform is specified, the level of spurious current unrelated to this waveform is specified, and the allowable variation in the amplitude of the module load current is also specified. The first two of these are specified below; specifications for the maximum variation in module load current are found in section 3.2.4.

RULE 8.1.2.1.1-1:

Module conducted emissions at harmonics of the 40 kHz power supply **MUST NOT** exceed the limits specified in figure 8-4. Where the limits of figure 8-4 fall below the limits of figure 8-5, the limits of figure 8-5 shall apply. The suggested test procedure for this requirement is described in section B.3.2.1.

OBSERVATION 8.1.2.1.1-2:

The amplitude of the 40 kHz square wave module load current can be approximated from:

$$I_{40\,kHz} \approx \frac{P}{24.3\ Volts}$$

where P is the specified module power consumption in watts.

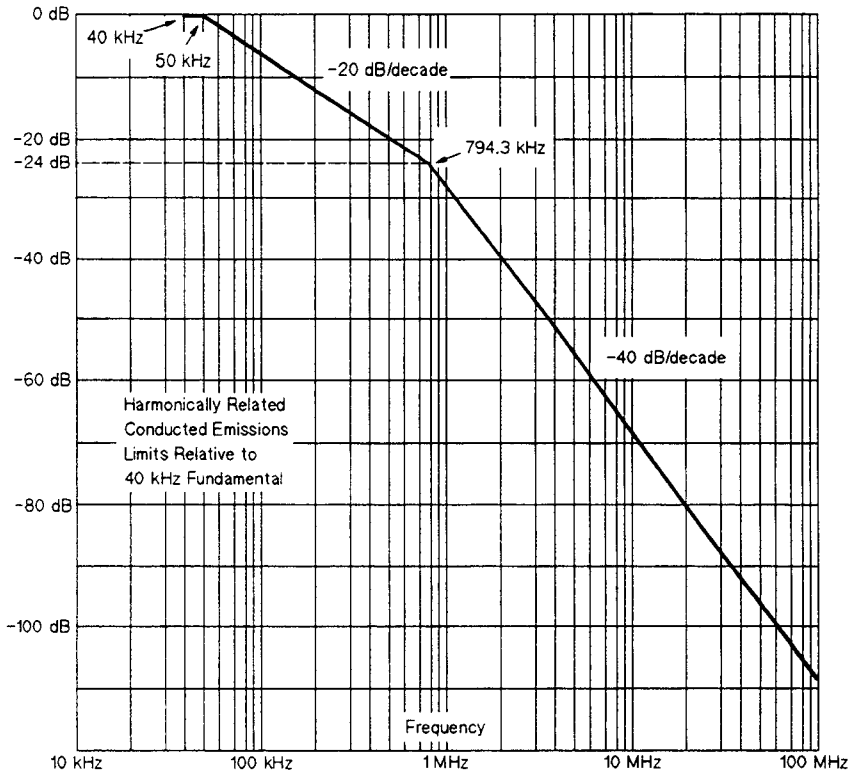

Figure 8-4. Module 40 kHz Harmonic Conducted Emissions Limits Relative to 40 kHz Current

RULE 8.1.2.1.1-3:

Module non-harmonic spurious emissions on the 40 kHz power bus are specified common mode on both phases of the 40 kHz power bus. These emissions **MUST NOT** exceed the limits specified in figure 8-5 The suggested test procedure for this requirement is described in section B.3.2.1.

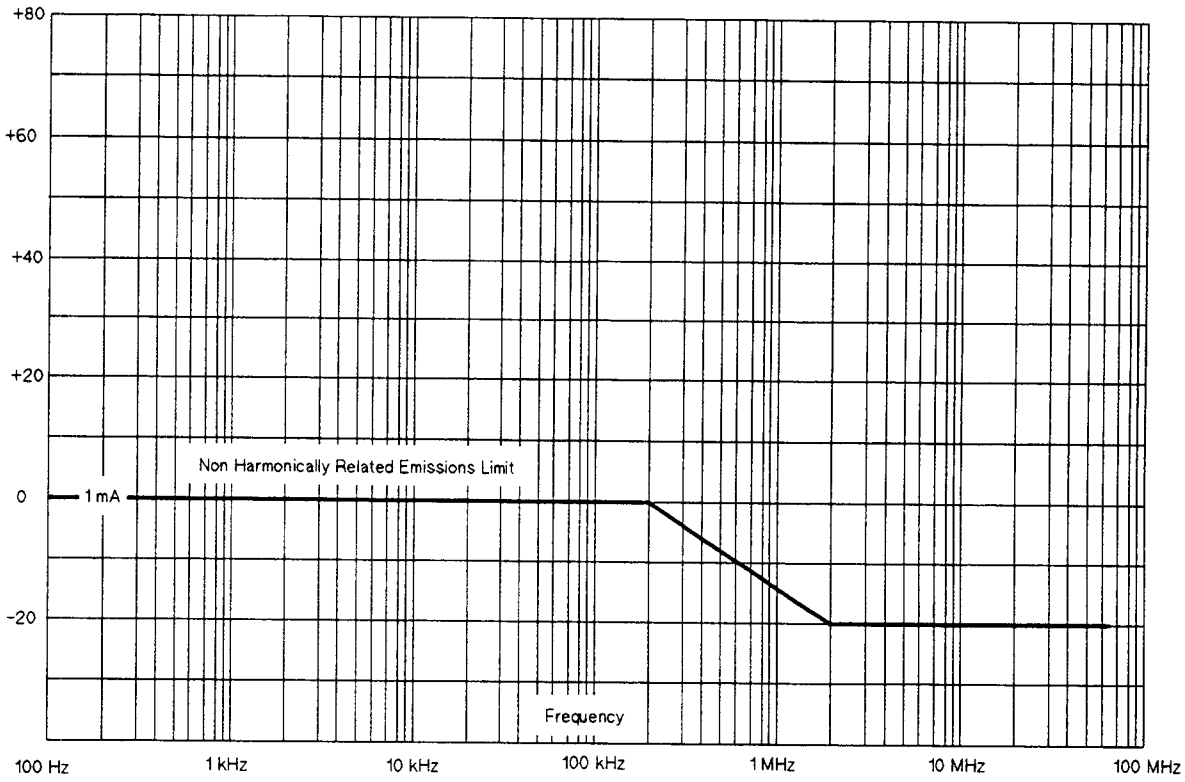

Figure 8-5. Module 40 kHz AC Supply Conducted Emissions Limits

RECOMMENDATION 8.1.2.1.1-4:

A common mode filter should be used on the power bus input lines to attenuate common mode emissions from a module. An example of an appropriate filter is shown in figure 8-6.

RULE 8.1.2.1.1-5:

Capacitors connected between line and ground on the 40 kHz power bus (such as are used in the conducted emissions filter in figure 8-6) **MUST** be less than 5000 pF.

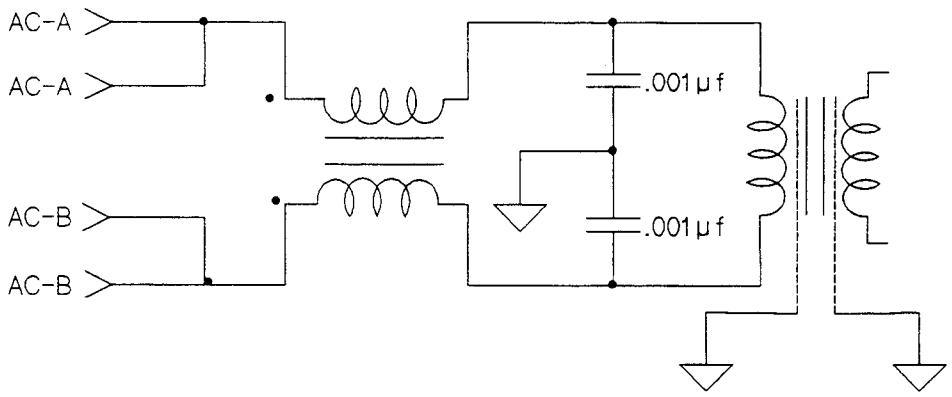

Figure 8-6. Common Mode Filter

OBSERVATION 8.1.2.1.1-6:

Experience indicates that capacitors in the range of 470 pF to 1000 pF tend to provide optimum performance.

8.1.2.1.2 Module Power Bus Conducted Susceptibility

The quality of the 40 kHz power supply available to a module can be degraded by other modules present in the same mainframe. A module must perform properly in the presence of this degradation. The levels of spurious signals on the power supply bus which a module must endure while meeting its specifications are given below.

RULE 8.1.2.1.2-1:

Modules **MUST** meet their specifications when subjected to voltage levels shown in figure 8-7 on either the AC-A or AC-B phases of the power supply. The suggested test procedure for this requirement is described in section B.3.2.2.

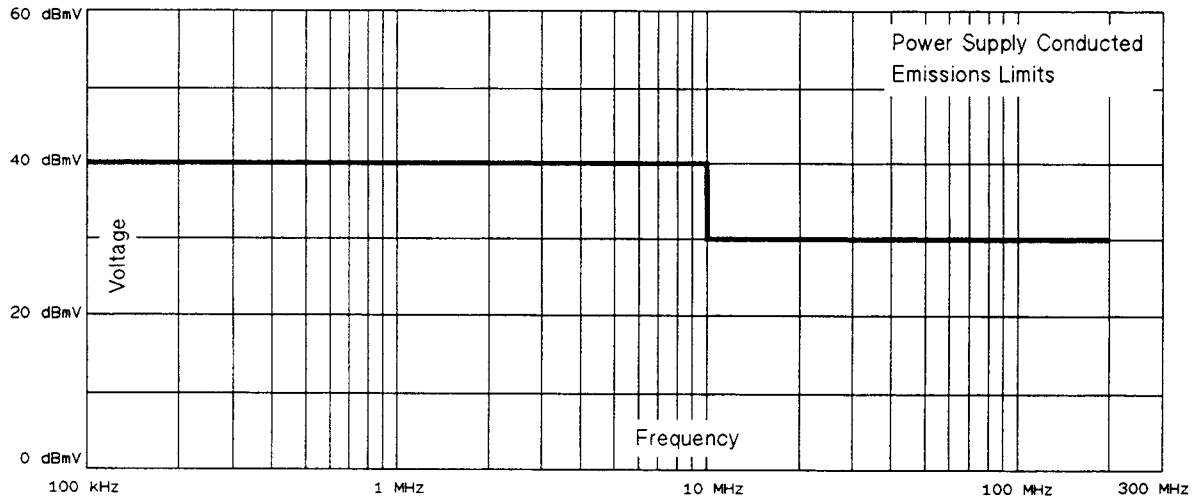

Figure 8-7. Module Power Supply Conducted Susceptibility Limit

8.1.2.2 Module Digital Bus Conducted EMC

The interaction between a module and the MSIB and IEEE-488.1 buses can be a cause of problems for that module or other modules on the bus. The fast edges of the logic signals present contain significant amounts of energy at high frequencies. There are two main ways in which these signals can cause EMC problems. First, they can degrade the performance of the mainframe, or the performance of modules in it. Second, they can radiate from the mainframe, causing it to tail its radiated emissions specifications.

RECOMMENDATION 8.1.2.2-1:

For many modules, highest radiated emissions levels are found when MSIB is active. For this reason, it is recommended that radiated emissions tests such as MIL-STD-461C RE02 be performed with the bus active at its maximum rate. This can be accomplished by implementing the busy-out function in module firmware. Details of this function are described in section 5.14.

8.1.2.2.1 Module Digital Bus Conducted Susceptibility

A module's performance can be affected by the traffic on MSIB. Even when a module is not actively using the bus, it is still electrically connected to it. Because of this, a module's performance can be affected by MSIB traffic even when that module is not actively using the bus. A module **MUST** be able to operate under these conditions

RULE 8.1.2.2.1-1:

Modules **MUST** meet their specifications when the MSIB is busied out. The bus is busied by placing another module in the same mainframe and invoking the busy-out function in that module.

SUGGESTION 8.1.2.2.1-2:

For purposes of consistency, it is suggested that the busy module used for the test in the previous rule be set to address 32 (row 1, column 0).

8.2 Mainframe Electromagnetic Compatibility

The following requirements apply to mainframes. The intent of these requirements is to assure electromagnetic compatibility between mainframes and modules. To that end, the focus of this specification is on the interfaces between mainframes and modules. Radiated emissions and susceptibility on the surface of the mainframe's module cavity are specified. Conducted emissions and susceptibility on the 40 kHz power bus and the IEEE-488.1 and MSIB buses are specified.

These requirements do not address electromagnetic interaction between modules and the external environment. Radiated emissions and susceptibility beyond the confines of a mainframe are not specified. Conducted emissions and susceptibility of a mainframe on the AC power line are not specified.

RECOMMENDATION 8.2-1:

MMS mainframe manufacturers should specify which regulator or other EMC standards they comply with.

OBSERVATION 8.2-2:

When assembling modules into mainframes, total system EMC will be a function of the particular modules, mainframes, and interconnecting cables used in the system. MMS system attributes allow this performance to fall into manageable limits.

8.2.1 Mainframe Radiated EMC

This specification does not dictate the particular set of regulatory EMC standards with which a mainframe must comply. It does not require adherence to, for example, FCC, VDE, or Mil Spec EMC requirements.

8.2.1.1 Mainframe Radiated Emissions

RECOMMENDATION 8.2.1.1-1:

If a mainframe manufacturer specifies compliance to a given set of regulatory EMC standards, it is recommended that the mainframe be tested individually, with no modules, to the limits of the specification. It is not necessary to derate the specification limit. The purpose of this recommendation is to ensure that EMC claims by different manufacturers have a common definition. This will ease the burden on system integrators who wish to design a system meeting specific regulatory EMC requirements.

OBSERVATION 8.2.1.1-2:

A system composed of multiple modules and mainframes may have radiated emissions levels higher than that of the mainframe when tested individually. If a system is to meet a given radiated emissions specification, the radiated emissions levels of the mainframe or mainframes may need to be lower.

RECOMMENDATION 8.2.1.1-3:

The design of the mainframe enclosure has a strong effect on the radiated emissions of a system. Proper grounding of modules is important if a system is to meet its standards for radiated emissions. For this reason, it is recommended that all mainframes use the module grounding scheme described in the MMS Mechanical Interface Specification drawing package.

In order to assure compatibility between modules and between modules and mainframes, near field magnetic emissions are specified in the mainframe's module cavity.

8.2.1.1.1 Mainframe Magnetic Field Radiated Emissions

RULE 8.2.1.1.1-1:

The close-field emissions measured on the surfaces of the module cavity **MUST NOT** exceed the limit shown in figure 8-1 The probe used to measure the magnetic field emissions **MUST** have an aperture of less than 100 mm^2. The suggested test procedure for this specification is described in section B.2.1.

8.2.1.1.2 Mainframe Electric Field Radiated Emissions

Near field electric field emissions are not specified. The accuracy of electric field measurements near metal surfaces is poor, and magnetic fields are a more severe threat in the module cavity.

8.2.1.2 Mainframe Radiated Susceptibility

In order to assure compatibility between mainframes and modules, near field magnetic susceptibility is specified in the module cavity.

8.2.1.2.1 Mainframe Magnetic Field Susceptibility

RULE 8.2.1.2.1-1:

The close field susceptibility measured on the surfaces of the mainframe's module cavity **MUST** be above the limit shown in figure 8-3. The probe used to generate the magnetic fields for this test **MUST** have an aperture of greater than 25 mm^2 . The suggested test procedure for this specification is described in section B.2.2.

8.2.1.2.2 Mainframe Electric Field Susceptibility

Near field electric field susceptibility is not specified. The accuracy of electric field measurements near metal surfaces is poor, and magnetic fields are a more severe threat in the module cavity.

8.2.2 Mainframe Conducted EMC

This specification does not dictate the particular set of regulatory EMC standards with which a mainframe must comply. It does not require adherence to, for example, FCC, VDE, or Mil Spec EMC requirements.

In order to assure compatibility between mainframes and modules, conducted emissions are specified at the module to mainframe backplane interface connector.

8.2.2.1 Mainframe Power Bus Conducted EMC

Mainframes deliver power to modules through the backplane interface connector. This power is delivered as a 40 kHz AC waveform, differentially balanced with respect to ground. In order to control interaction between modules and between modules and mainframes, mainframe conducted emissions and susceptibility are specified.

8.2.2.1.1 Mainframe Power Bus Conducted Emissions

The mainframe power supply output is nominally a 40 kHz AC waveform with an average value of 24.3 volts. Harmonic content and spurious signal levels are specified for the power supply output. The maximum level of ripple on the power supply output is also specified; this is specified in section 3.1.

8.2.2.1.1.1 Mainframe Power Supply Harmonics

RULE 8.2.2.1.1.1-1:

The 40 kHz mainframe power supply voltage waveform spectrum **MUST** comply with the limits of figure 8-8 when presented with any legal module load.

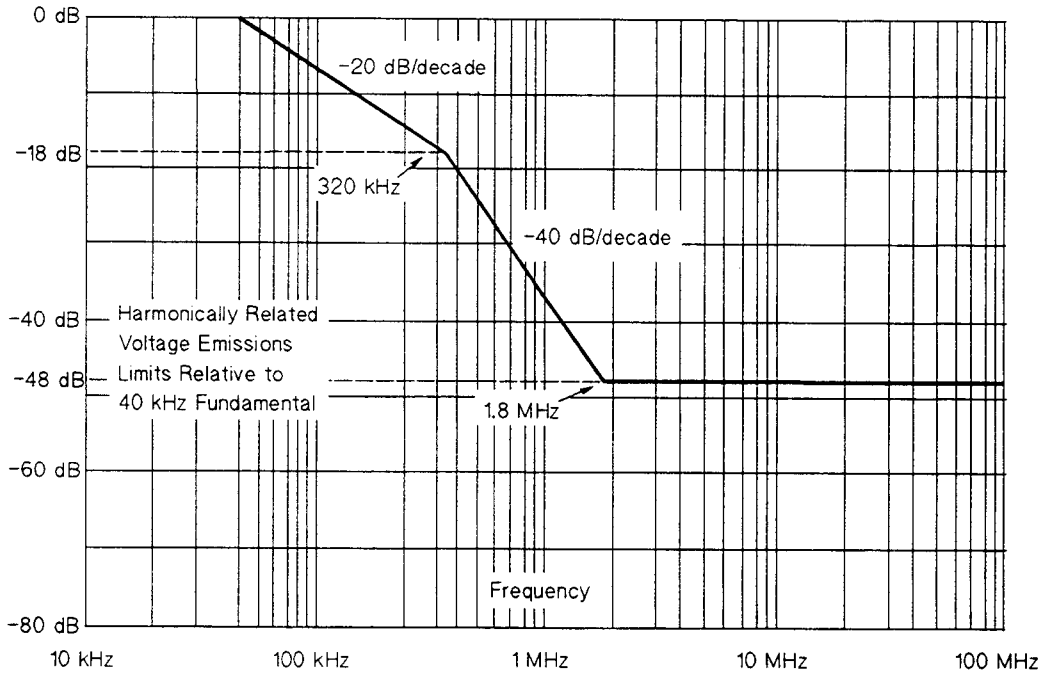

Figure 8-8. Mainframe 40 kHz Harmonic Emissions Limits Relative to 40 kHz Voltage

RULE 8.2.2.1.1.1-2:

The current waveform spectrum from the mainframe into any legal module load **MUST** comply with the limits imposed by figure 8-4 when delivering power in the range from 20 watts to the maximum rated output of the 40 kHz mainframe power supply.

8.2.2.1.1.2 Mainframe Power Supply Non-harmonic Emissions

Spurious signals on the mainframe power supply output are measured common mode on AC-A and AC-B with respect to ground. Common mode spurs are typically much higher than differentially-induced ones, as well as being easier to measure at low levels.

RULE 8.2.2.1.1.2-1:

The level of non-harmonic common mode emissions on the mainframe power bus **MUST NOT** exceed the limits of figure 8-9. The suggested test procedure for this requirement is described in section B.3.1.1.3.

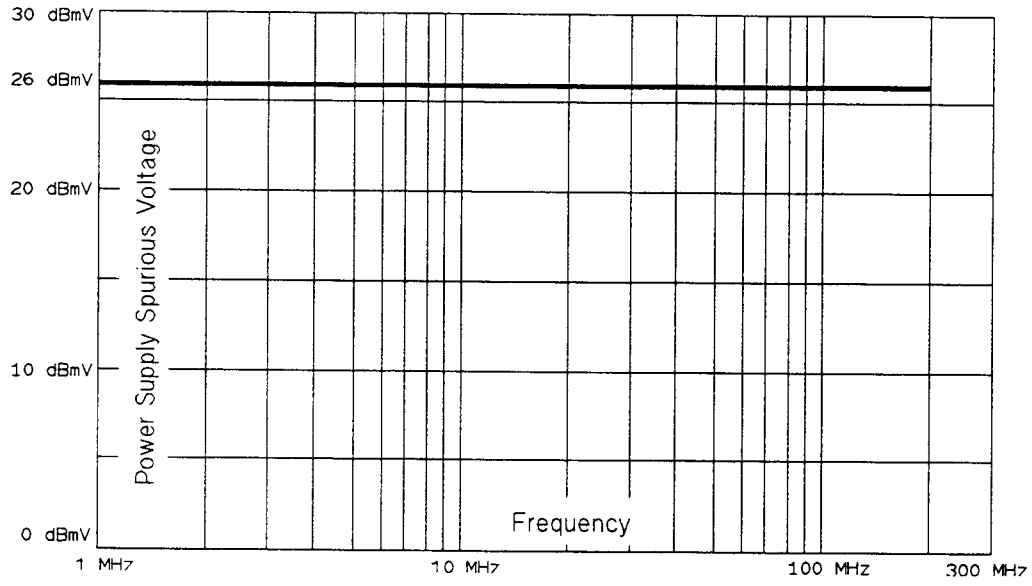

Figure 8-9. Mainframe Non-harmonic Common Mode Emissions

8.2.2.1.2 Mainframe Power Bus Conducted Susceptibility

The quality of the mainframe's power supply can be degraded by the modules that are connected to the power supply bus. If the impedance of the mainframe power supply is not controlled, modules could interact with each other through the common impedance of the power supply bus. These specifications are designed to limit the potential for this type of interaction.

8.2.2.1.2.1 Mainframe Power Supply Harmonic Susceptibility

The load current drawn by modules from the mainframe power supply is nominally a square wave. The spectrum of this square wave consists of a broad spectrum of high level harmonics. It is necessary to measure the voltage harmonics induced on the power supply output when subjected to these large current harmonics which are present.

RULE 8.2.2.1.2.1-1:

The large-signal impedance of the mainframe power supply **MUST NOT** exceed the limits of figure 8-10. This is measured under full load conditions at odd harmonics of the fundamental power supply frequency. The suggested test procedure for this requirement is described in section B.3.1.2.1.

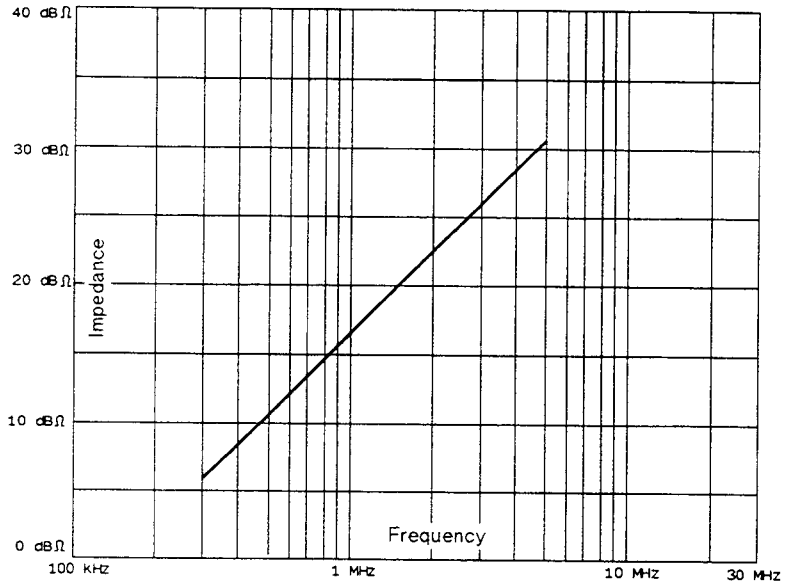

Figure 8-10. Mainframe Harmonic Impedance

8.2.2.1.2.2 Mainframe Power Supply Non-Harmonic Susceptibility

This test measures the susceptibility of the mainframe power supply to spurious currents injected onto the power bus by modules. For this test, the currents are injected into AC-A and AC-B common mode with respect to ground.

RULE 8.2.2.1.2.2-1:

The common mode impedance of the mainframe power supply **MUST NOT** exceed the limits of figure 8-11. The suggested test procedure for this requirement is described in section B.3.1.2.2.

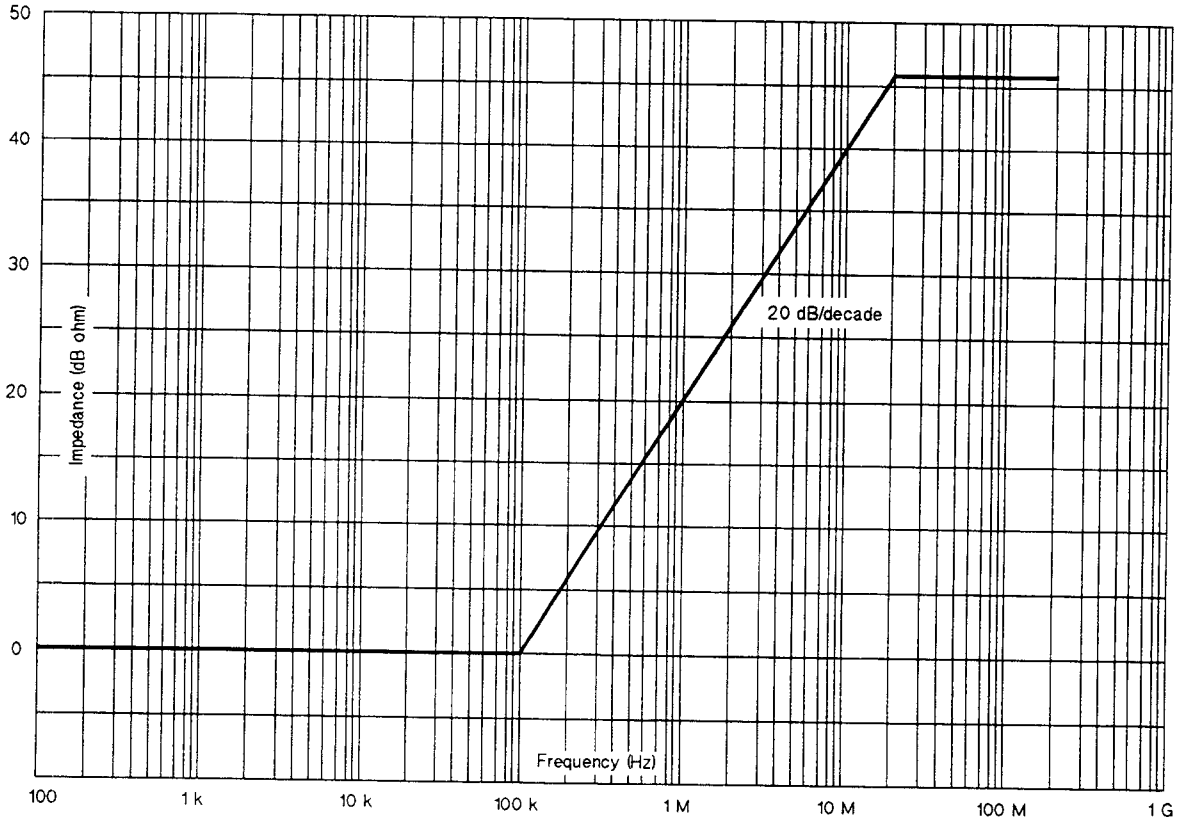

Figure 8-11. Mainframe Common Mode Output Impedance

8.2.2.2 Mainframe Digital Bus Conducted EMC

The interaction between a mainframe and the MSIB and IEEE-488.1 buses can be a cause of problems for that mainframe or for modules in it. The fast edges of the logic signals present contain significant amounts of energy at high frequencies. There are two main ways in which these signals can cause EMC problems. First, they can degrade the performance of the mainframe, or the performance of modules in it. Second, they can radiate from the mainframe, causing it to fail its radiated emissions specifications.

8.2.2.2.1 Mainframe Digital Bus Conducted Susceptibility

A mainframe's performance can be affected by the traffic on MSIB. Even when a mainframe is not actively using the data bus, it is still electrically connected to it. Because of this, a mainframe's performance can be affected by MSIB traffic even when the mainframe itself is not sending or receiving data. A mainframe **MUST** be able to operate under these conditions.

RULE 8.2.2.2.1-1:

Mainframes **MUST** meet their specifications when the MSIB is busied out. The bus is busied by placing a module in the mainframe and invoking the busy-out function in that module. Details of the busy-out function are described in section 5.14.

SUGGESTION 8.2.2.2.1-2:

For purposes of consistency, it is suggested that the busy module used for the above test be set to address 32 (row 1, column 0).

9. CAPABILITY LABELING

MMS mainframes and modules are labeled to provide the MMS system integrator with the information needed to configure a system.

9.1 Module Labeling

RULE 9.1-1:

An MMS module **MUST** have capability labeling on its module front, with the module power requirement in watts and the module cooling requirement per slot in liters per second.

SUGGESTION 9.1-2:

It is desirable that module capability labeling be located in a consistent location. Figure 6-67 shows the suggested location.

PERMISSION 9.1-3:

The module capability labeling **MAY** be hidden in normal operation (e.g. behind a door or panel), provided the user can easily access the label from the front of the module.

9.2 Mainframe Labeling

RULE 9.2-1:

An MMS mainframe **MUST** have capability labeling which gives the total power available to modules in watts, and the minimum airflow per mainframe slot in liters per second.

RULE 9.2-2:

The mainframe capability labeling **MUST** be readable from the front of the mainframe.

PERMISSION 9.2-3:

The mainframe capability labeling **MAY** be hidden in normal operation (e.g. behind a door or panel), provided the user can easily access the label from the front of the mainframe.

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A. CONNECTOR PIN DESCRIPTIONS

A.1 MSIB Internal Connector

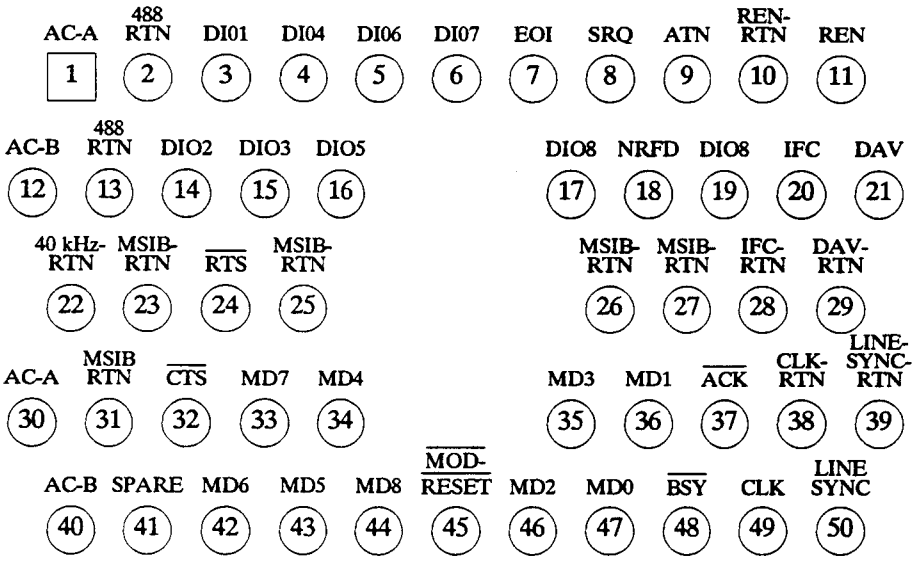

Figure A-1. 50 Pin Module Connector (View of Mating Face on Mainframe)

TABLE A-1. Pin Assignments for 50 Pin Module Connector

Pin	Assignment	Pin	Assignment	Pin	Assignment
1	AC-A	12	AC-B	22	40 kHz-RTN [3]
2	488 RTN [1]	13	488 RTN [1]	23	MSIB-RTN [1]
3	DI01	14	DI02	24	$\overline{\text{RTS}}$
4	DI04	15	DI03	25	MSIB-RTN
5	DI06	16	DI05	26	MSIB-RTN
6	DI07	17	DI08	27	MSIB-RTN [1]
7	E01	18	NRFD	28	IFC-RTN
8	SRQ	19	NDAC	29	DAV-RTN
9	ATN	20	IFC		
10	REN-RTN [1]	21	DAV		
11	REN				

Pin	Assignment	Pin	Assignment
30	AC-A	40	AC-B
31	MSIB RTN	41	SPARE [1]
32	$\overline{\text{CTS}}$	42	MD6
33	MD7	43	MD5
34	MD4	44	MD8
35	MD3	45	$\overline{\text{MOD-RESET}}$
36	MD1	46	MD2
37	$\overline{\text{ACK}}$	47	MD0
38	CLK-RTN [1]	48	$\overline{\text{BSY}}$
39	LINE-SYNC-RTN [2]	49	CLK
		50	LINE SYNC [4]

[1] These pins are connected to chassis ground in the mainframe. Connection to all returns must be made in the module for the respective bus (IEEE 488.1 and/or MSIB) as part of keeping electromagnetic emissions within specifications.

[2] Do not connect directly to module ground. Any module of one slot width using the LINE SYNC function needs to maintain a minimum of 20Ωs between LINE SYNC RETURN and module ground. A two slot module is 10Ωs minimum and a three slot module is 6.7Ωs minimum.

[3] Pin 22 is to be used for grounding of cable shield drain wire when a separate 40 kHz power cable is used. Module 40 kHz RFI filter returns may also connect to this pin provided they are kept separate from all other module returns and grounds.

[4] Any one slot module using the LINE SYNC function needs to present an impedance of 100 kΩ or greater to the mainframe. A two slot module is 50 kΩs minimum and a three slot module is 33 kΩs minimum.

A.2 MSIB External Connector

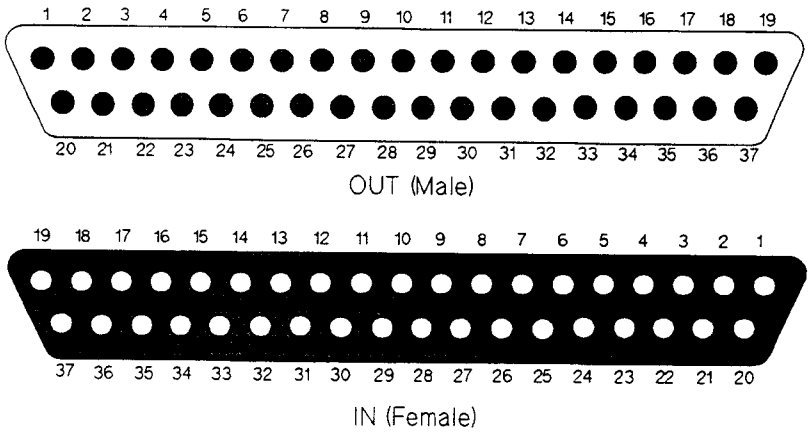

Figure A-2. MSIB External Connector

TABLE A-2. Pin Assignments for MSIB External Connector

Pin	Assignment	Pin	Assignment
1	D0L	20	D0H
2	D1L	21	D1H
3	D2L	22	D2H
4	D3L	23	D3H
5	D4L	24	D4H
6	D5L	25	D5H
7	D6L	26	D6H
8	D7L	27	D7H
9	D8L	28	D8H
10	FR1L	29	FR1H
11	FR0L	30	FR0H
12	DAVL	31	DAVH
13	DACL	32	DACH
14	RESET	33	GND
15	GND	34	SRDY
16	GND	35	CABLE
17	GND	36	GND
18	GND	37	DRDY
19	CGND		

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B. MEASUREMENT TESTS

B.1 Power Supply Electrical Tests

Module power consumption is dynamic. It can vary with the state of the module. For example, it may vary as the frequency of a YIG tuned oscillator is varied. For some modules, it may exhibit transient peaks. Modules with mechanical switches and attenuators, for example, will draw more current from the power supply when those switches' relays are activated.

For this reason, the module power consumption test has two parts. The first test, described in section B.1.1.1, measures the steady state power drawn by a module from the 40 kHz power supply. This test, which measures power consumption over a span of several seconds, will be sufficient for modules that do not exhibit large transient peaks in power consumption. The second test, described in section B.1.1.2, measures the additional power drawn from the mainframe power supply during transients. This test should be run along with the first on modules expected to exhibit transient peaks in their power consumption.

B.1.1 Module Power Consumption Tests

B.1.1.1 Module Steady State Power Consumption Test

B.1.1.1.1 Description

This test procedure is intended to test the power consumption of MMS modules. The measurement is necessary for the module designer to guarantee compliance with the MMS specification. Because of the nature of the power supplies, the power measurement is not a straight forward measurement of voltage and current ($V \times I = P$). The measurement must be made by sampling both the voltage and current, and then integrating. The method used was chosen for several reasons:

1. The power supply voltage is distributed differentially and is balanced with respect to ground,
2. The power supply distribution system operates at 40 kHz,
3. The modules present non-linear loads resulting in a non-sinusoidal current waveform which is typically approaching a square wave which produces many harmonics,
4. Typical wattmeters and voltmeters are unable to accurately measure the power consumed by a module because the frequencies involved are higher than the meters can measure.

The method developed to measure power requires sampling two voltages. The first voltage is the 40 kHz power bus. The second voltage is a function of the current on the 40 kHz power bus. The sampling process involves sampling 250 cycles of each voltage, first the bus voltage and then the voltage representing the current. The computer performs the necessary math, including integration, with the result being a plot of the power waveform and the average power.

The sampling process uses a trigger circuit to mark the same starting point on each cycle. The voltmeter waits a given delay before taking the sample. With each sampling the delay is increased until the whole waveform is represented. This is approximately 250 cycles. This is then repeated for the current waveform. The result is 250 pairs of points, one voltage and one current. The two points of each pair are multiplied together, voltage times current. The result is 250 power points. The sum of all the power points is divided by 250 to determine the average power.

The software corrects for frequency variations in the 40 kHz power bus so that the average power is for one complete cycle.

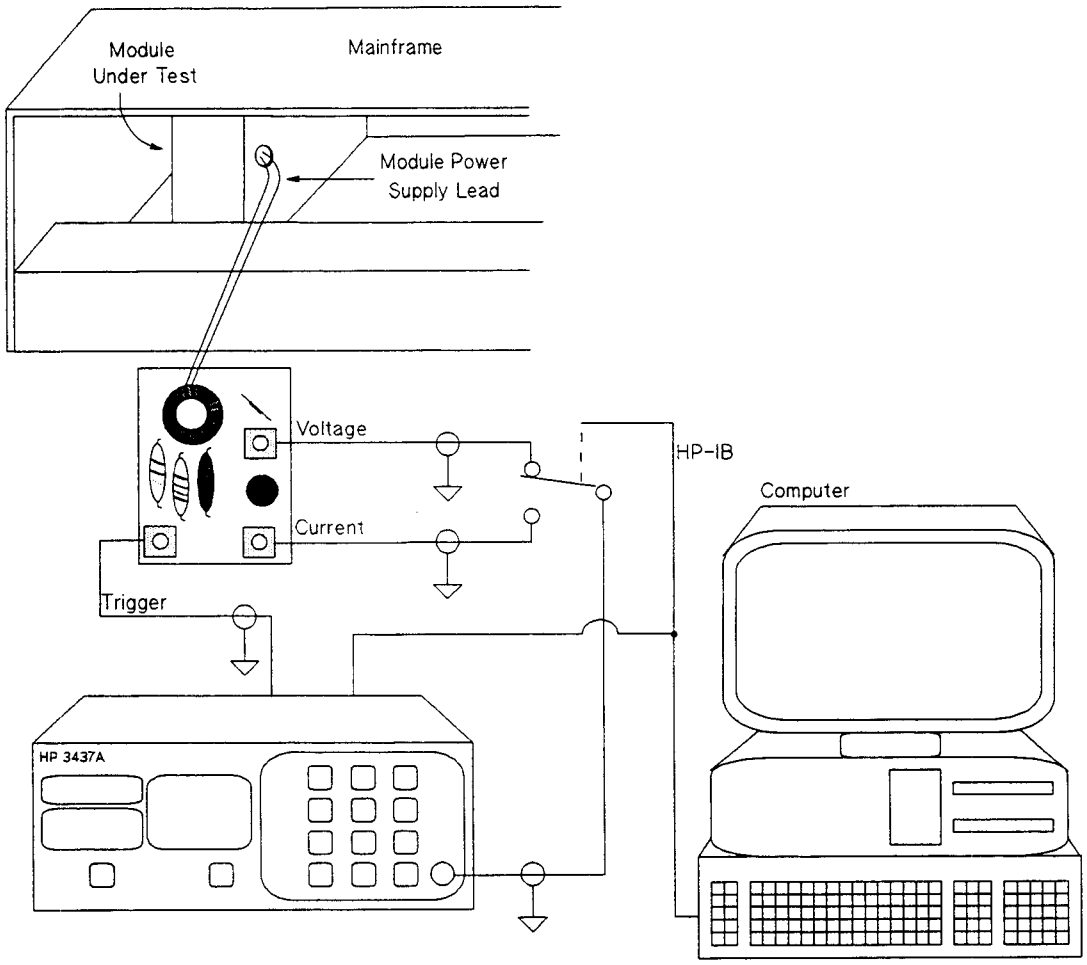


Figure B-1. Power Measurement Block Diagram

Connect the cables as shown in figure B-1. The module's power supply current can be measured at the module fuse. If there is more than one fuse on either side of the 40 kHz AC line, the power down each leg of one side of the 40 kHz line will have to be measured. The total module power can then be calculated by taking the sum of each of the legs. These are the fuses on the primary side of the module power transformer.

The module under test should be put into the state that draws the most current/power from the 40 kHz line before running the test. An example would be a module that uses a magnetically tuned oscillator or filter such as YIG oscillator or YIG tuned filter. These devices require considerably more current when tuned to the maximum frequency.

B.1.1.1.2 Equipment

- Power probe electronic tool,
- system voltmeter (e.g., HP 3437A),
- VHF switch (e.g., HP 3488A),
- MMS Mainframe (e.g., HP 70001A),
- Plotter/Printer,
- Computer,
- Computer Software.

B.1.1.1.3 Procedure

1. Configure test setup. Refer to block diagram in figure B-1.
2. Run the measurement program.
3. Review results/data.

B.1.1.1.4 Software

The following software program can be used to measure the average power consumption of modules, using the measurement setup of figure B-1. It is included here to aid users in developing their average power measurement procedure. The software is written in Hewlett-Packard BASIC 3.0.

```
10    ! This program measures the power consumption of an MMS module.
20    ! It measures the 40 kHz power supply voltage and the 40 kHz
30    ! current drawn by the module.  A switch is used to select between
40    ! the two signals.  A sampling voltmeter samples several cycles of
50    ! both signals.  The program then integrates the product of the
60    ! voltage and the current, and calculates the power consumed by
70    ! the module.
80    !
90    ! 250 samples are taken of both the voltage and current waveforms.
100   ! A trigger circuit is used to generate a stable timing reference
110   ! from the 40 kHz power supply voltage.  This trigger is used to
120   ! trigger the sampling voltmeter's measurement.  The voltmeter has
130   ! a programmable delay which allows the user to program in a delay
140   ! between the time when the trigger occurs and the time when the
150   ! measurement is made.  After each measurement is made, this
160   ! program increments the programmable delay.  This way, repeated
170   ! measurements at increasing delays successively build up a
180   ! sampled representation of the entire waveform.  Enough samples are
190   ! taken to acquire two complete cycles of both the voltage and the
200   ! current.  The array of sampled data is then truncated so that
210   ! exactly one cycle of the voltage and current is used for the
220   ! power calculation.
230   !
240   ! The program then calculates the average power consumption over
250   ! one cycle, and displays the results.
260   !
270   ! This is a working sample program and it is the
271   ! end users responsibility to modify, store and display the data in their
272   ! desired format.
280   ! ********** INITIALIZE **********
290   GCLEAR
300   Voltmeter=724                    ! Hpib address voltmeter
310   Switch=709                       ! Hpib address switch.
```

```
320   DIM Voltage_a(600),Current_a(600)
330   !
340   INTEGER Num_readings,First_loc,Last_loc,New_last_loc,Dvm_delay,Ctr,X
350   INTEGER Max_2cycle_pts,Select_code,Last_command
360   REAL V_scale_factor,I_scale_factor,Correction,Isum_sqrs,Vsum_sqrs
370      !
380   Max_2cycle_pts=530  !assures two complete cycles.
390   Num_readings=SIZE(Voltage_a,1)
400   First_loc=BASE(Voltage_a,1)
410   Last_loc=First_loc+Num_readings-1
420      !
430   OUTPUT Switch;"CRESET 1,2,3,4,5"
440   OUTPUT Switch;"CLOSE 100"
450   WAIT .3
460   !
470   ! *************** MEASURE V ***************
480   !
490   Dvm_delay=235           ! Initial delay.
500   V_scale_factor=11.0     ! Multiplier for voltage measurement.
510       !
520   ALLOCATE Meas_v(First_loc:Last_loc)
530       !
540   OUTPUT Voltmeter;"R2,T2,F1"
550       !
560   FOR Ctr=First_loc TO Last_loc
570   OUTPUT Voltmeter USING """D"",.7D,""S""";(Dvm_delay+Ctr)*1.E-7
580   ENTER Voltmeter;Meas_v(Ctr)
590   NEXT Ctr
600 !
610 !
620   ! *************** MEASURE I ***************
630   OUTPUT Switch;"CRESET 1,2,3,4,5"
640   OUTPUT Switch;"CLOSE 101"
650   WAIT .1
660   Dvm_delay=235
670   I_scale_factor=2.5            ! Multiplier for Current
680   ALLOCATE Meas_i(First_loc:Last_loc)
690   OUTPUT Voltmeter;"R2,T2,F1"
700   FOR Ctr=First_loc TO Last_loc
710   OUTPUT Voltmeter USING """D"",.7D,""S""";(Dvm_delay+Ctr)*1.E-7
720   ENTER Voltmeter;Meas_i(Ctr)
730   NEXT Ctr
740 !
750   !xxxxxxxxxxxxxxxxxx SCALE v xxxxxxxxxxxxxxxxxxx
760   !
770   MAT Voltage_a= Meas_v*(V_scale_factor)
780       !
790   New_first_loc=First_loc
800   WHILE Voltage_a(New_first_loc)<0     ! Find start of wave cycle.
810   New_first_loc=New_first_loc+1
820   END WHILE
830       !
840   New_last_loc=New_first_loc+Max_2cycle_pts
850   WHILE Voltage_a(New_last_loc-1)>=0   ! Find end of 2 complete cycles.
860   New_last_loc=New_last_loc-1
870   END WHILE
880       !
890   Num_pts=New_last_loc-New_first_loc+1
900   ALLOCATE Voltage(1:Num_pts)
910   ALLOCATE V_a(1:Num_pts)
920   FOR I=New_first_loc TO New_last_loc  ! Fill array with 2 cycles.
930   V_a(I-New_first_loc+1)=Voltage_a(I)
940   NEXT I
950   !
960   !
970   MAT Voltage_a= (0)                   ! Clean out array, set to 0.
```

```
980   REDIM Voltage_a(1:Num_pts)           ! Prefare array to receive final data
990   MAT Voltage_a= V_a                   ! Store data of 2 complete cycles.
1000  !
1010  !xxxxxxxxxxxxxxxxx SCALE i xxxxxxxxxxxxxxxxxxx
1020  !
1030  INPUT "mat number",Z
1040  MAT Meas_i= (2*Z/2.5)
1050  IF 2.5*MAX(Meas_i(*))/2>4 THEN       ! If I is > 4 amps use correction
1060  INPUT "ENTER percentage of unregulated load",Probe_error
1070  FOR Error=First_loc TO Last_loc
1080 Meas_i(Error)=Meas_i(Error)*(1+(Probe_error/100)*(ABS(.04*Meas_i(Error))/(27-ABS(Meas_i(Error)))))
1090  NEXT Error
1100  END IF
1110  MAT Current_a= Meas_i*(I_scale_factor)
1120  ALLOCATE Current(1:Num_pts)
1130  ALLOCATE C(1:Num_pts)
1140  FOR I=New_first_loc TO New_last_loc
1150  C(I-New_first_loc+1)=Current_a(I)
1160  NEXT I
1170  MAT Current_a= (0)
1171  REDIM Current_a(1:Num_pts)
1172  MAT Current_a= C
1173  !
1181  ! XXXXXXXXXXXX voltage calcs XXXXXXXXXXXXXXXXXX
1185  !
1190  ALLOCATE Temp(1:Num_pts)
1210  ALLOCATE Q(1:Num_pts)
1220  MAT Voltage= (2)*Voltage_a
1221  Vpk=MAX(Voltage(*))
1230  PRINT "Vpk";Vpk
1240  !
1250  MAT Temp= Voltage . Voltage
1260  Vsum_sqrs=SUM(Temp)              ! Calculate Vrms.
1270  Vrms=SQR(Vsum_sqrs/Num_pts)      !      "
1280  PRINT "Vrms";Vrms
1290  MAT Temp= Voltage
1300  MAT Q= Temp<(0)
1310  MAT Q= Q*(-2)
1320  MAT Q= Q+(1)
1330  MAT Temp= Temp . Q
1340  Vavg=SUM(Temp)/Num_pts           ! Calculate V average.
1350  PRINT "Vavg";Vavg
1360       !
1370  !  xxxxxxxxxxxxxxxxxxx current calcs xxxxxxxxxxxxxx
1380  MAT Current= Current_a
1390  Ipk=MAX(Current(*))
1400  PRINT "Ipk";Ipk
1410  MAT Temp= Current . Current
1420  Isum_sqrs=SUM(Temp)
1430  Irms=SQR(Isum_sqrs/Num_pts)
1440  PRINT "Irms";Irms
1450  MAT Temp= Current
1460  MAT Q= Temp<(0)
1470  MAT Q= Q*(-2)
1480  MAT Q= Q+(1)
1490  MAT Temp= Temp . Q
1500  !
1510  Iavg=SUM(Temp)/Num_pts
1520  PRINT "Iavg";Iavg
1530  !
1540  !xxxxxxxxxxxxxxxx power calculations xxxxxxxxxxxxxxxx
1550  !
1560  DIM Power(600)
1570  REDIM Power(1:Num_pts)
1580  MAT Power= Voltage . Current
1590  Pavg=SUM(Power)/Num_pts
```

```
1600  Ppk=MAX(Power(*))
1610  PRINT "Pavg";Pavg
1620  PRINT "Ppk";Ppk
1630  !
1640  ! xxxxxxxxxxxxxx initialize graphics xxxxxxxxxxxxxxxxx
1650  !
1660  INTEGER I
1670     !
1680  GINIT
1690  VIEWPORT 10,120,45,85
1700  DEG
1710  GRAPHICS ON
1720  PEN 1
1730  CSIZE 3,.65
1740  !
1750  ! xxxxxxxxxxxxxx current graph xxxxxxxxxxxxxxxxxxxxxx
1760  !
1770  ALPHA OFF
1780  Imax=2
1790  INPUT "Module width",Module_width
1800  ALPHA OFF
1810  WINDOW 0,Num_pts,-Imax*Module_width,Imax*Module_width
1820   LINE TYPE 1
1830   AXES Num_pts/8,.5*Module_width,Num_pts,0,2,1
1840   CLIP OFF
1850   LORG 2
1860   FOR Y_val=-Imax*Module_width TO Imax*Module_width STEP .5*Module_width
1870   MOVE Num_pts+5,Y_val
1880   LABEL Y_val
1890   NEXT Y_val
1900   MOVE Num_pts,(Imax+.1)*Module_width
1910   LORG 7
1920   LABEL "CURRENT (Amps)"
1930   CLIP ON
1940   LINE TYPE 4
1950   MOVE 0,Current(1)
1960   FOR I=1 TO Num_pts
1970   PLOT I,Current(I)
1980   NEXT I
1990      !
2000  !
2010  WAIT 2
2020  ! xxxxxxxxxxxxxxxx voltage graph xxxxxxxxxxxxx
2030  !
2040  Vmax=50
2050  WINDOW 0,Num_pts,-Vmax,Vmax
2060  LINE TYPE 1
2070  AXES Num_pts/8,10,0,0,2,1
2080  CLIP OFF
2090  LORG 8
2100  FOR Y_val=-Vmax TO Vmax STEP 10
2110  MOVE 0,Y_val
2120  LABEL Y_val
2130  NEXT Y_val
2140  MOVE 0,V_max
2150  LORG 1
2160  LABEL "VOLTAGE (VOLTS)"
2170  CLIP ON
2180  LINE TYPE 5
2190  MOVE 0,Voltage(1)
2200  FOR I=1 TO Num_pts
2210  PLOT I,Voltage(I)
2220  NEXT I
2230  WAIT 2
2240  !
2250  ! xxxxxxxxxxxxxxxx power graph xxxxxxxxxxxxxxxx
```

```
2260   !
2270   Pmax=30
2280   WINDOW 0,Num_pts,-Pmax*Module_width,Pmax*Module_width
2290   LINE TYPE 1
2310 ! IPLOT 0,Pmax*Module_width,-1
2320   CLIP OFF
2330 ! FOR Y_val=5*Module_width TO Pmax*Module_width STEP 5*Module_width
2340 ! MOVE Num_pts/2,Y_val
2350 ! IPLOT 4,0,-1
2360 ! NEXT Y_val
2370   LORG 8
2380   FOR Y_val=10*Module_width TO Pmax*Module_width STEP 10*Module_width
2390   MOVE Num_pts/1,Y_val
2400   LABEL Y_val
2410   NEXT Y_val
2420   MOVE Num_pts/2,(Pmax+5)*Module_width
2430   LORG 4
2440   LABEL "POWER (Watts)"
2450   CLIP ON
2460   LINE TYPE 1
2470   MOVE 0,Power(1)
2480   FOR I=1 TO Num_pts
2490   PLOT I,Power(I)
2500   NEXT I
2510   !
2520   ! xxxxxxxxxxxxxx print data labels xxxxxxxxxx
2530   !
2540   VIEWPORT 1,133,1,45
2550   WINDOW 1,80,15,1
2560   CSIZE 3.5,.6
2570   LORG 2
2580 Fmt1:    IMAGE 3X,15A,DD.DD,X,A,9X,16A,DD.DD,X,A
2590 Fmt2:          IMAGE 3X,9A,22X,13A
2600 Fmt3:              IMAGE 17X,14A,DD.DD,X,5A
2610   MOVE 1,4
2620   LABEL USING Fmt3;"AVERAGE PWR = ",Pavg,"WATTS"
2630   MOVE 1,7
2640   LABEL USING Fmt1;"RMS VOLTAGE  = ",Vrms,"V","RMS CURRENT   = ",Irms,"A"
2650   MOVE 1,9
2660   LABEL USING Fmt2;"""AVERAGE""","EQUIV. SQUARE"
2670   MOVE 1,10
2680   LABEL USING Fmt1;" VOLTAGE     = ",Vavg,"V"," WAVE CURRENT = ",Pavg*PI/80,"A"
2690   MOVE 1,12
2700   LABEL USING Fmt1;"PEAK VOLTAGE = ",Vpk,"V","PEAK CURRENT  = ",Ipk,"A"
2710   PENUP
2720     !
2730     ALPHA OFF
2740     PAUSE
2750     END
```

B.1.1.1.5 Power Probe Electronic Tool Documentation

B.1.1.1.5.1 General Description

The power probe electronic tool provides a convenient and accurate means of measuring the power consumption of the module that is being tested.

The power probe electronic tool has an input and three outputs. The input is the primary side of a transformer which is connected in series with either the "AC-A" or the "AC-B" side of the 40 kHz bus. The transformer is used to convert the current into a voltage that is directly proportional to the current.

The other two outputs are voltage and a trigger circuit. The voltage output scales the 40 kHz bus voltage using a resistive divider. The third output is a trigger circuit that marks the start of each cycle.

B.1.1.1.5.2 Schematic

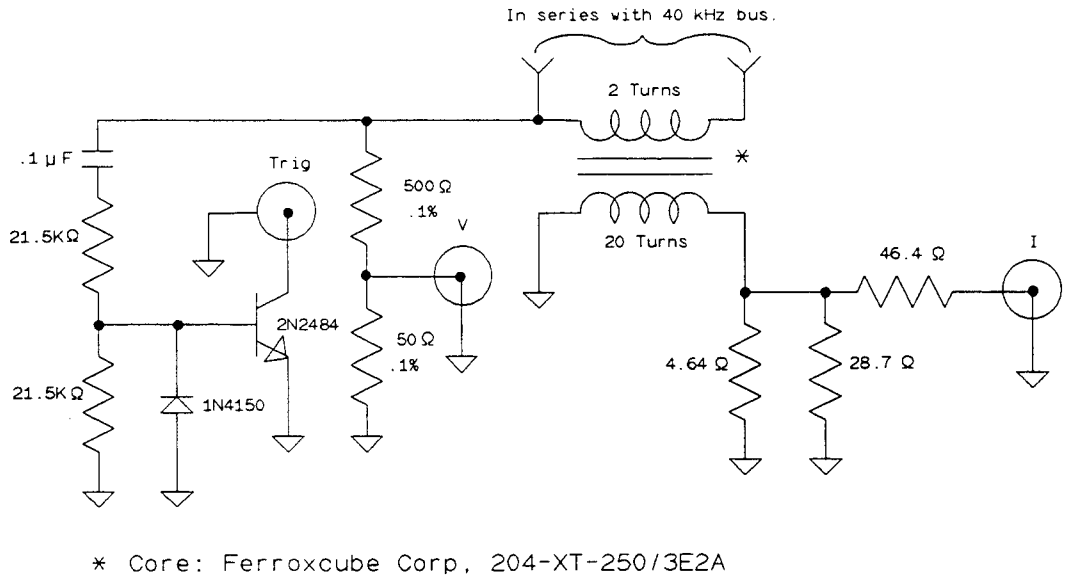


Figure B-2. Power Probe Electronic Tool

B.1.1.1.5.3 Schematic Notes

The power probe electronic tool will be processing currents up to 4 amperes. Therefore, when building the power probe electronic tool it is important to minimize contact resistance and wiring resistance. Shorter and larger wire should be used to minimize the resistance in the construction of the power probe electronic tool.

B.1.1.1.5.4 Functional Verification

Functional Verification of current probe: the voltage output and the current output (scaled in volts) need to be verified.

Place a 10 ohm, 1 %, 500 watt resistor across the output of the 40 kHz bus. The 10 ohm resistor can be realized by placing ten 100 ohm 50 watt resistors in parallel. This resistor needs to be a low inductance resistor with a good temperature coefficient. Resistors can be special ordered from C.T. Gamble, Debonco, New Jersey. The specifications are as follows: wire wound, 100 ohm, 1%, inductance < 1μ Henry, temperature coefficient < 20 ppm/degree centigrade.

Caution: This load dissipates 73 watts. A heat sink must be used to dissipate the heat and prevent the possibility of a burn.

Connect the input of the electronic tool in series with the resistive load. With the load in place, measure the voltage at the output labeled current using a voltmeter.

Note: This measurement can only accurately be made with a resistive load in place.

The voltage at the current output should measure 1.080 volts RMS +/- 2%, (1% load and 1% mainframes 27 VAC tolerances). The 1% error of the mainframe can be removed by calibrating the mainframe to its nominal value 24.3 volts average. The sensitivity of the current output is 2.50 amps/volt.

To verify the voltage output, connect the voltmeter to the voltage output. The voltage will be slightly less than 1.2273 volts RMS +/- 1% (1% mainframe's 27 VAC tolerance). 1.2273 volts is the no load voltage. The loaded voltage will be slightly smaller because of the connector and wiring resistance.

Note: The backplane interface connector's resistance is rated at 8.3 mΩ per contact maximum. Wiring resistance and inductance are a function of the size and length of wire used.

B.1.1.2 Module Transient Power Consumption Test

This test measures the increase in a module's power consumption when a dynamic event occurs. An example of this would be the spike in module power consumption occurring when a module draws a spike of current to drive a relay. The load current drawn by the module is measured on a spectrum analyzer. The spectrum analyzer is set to the frequency of the 40 kHz power supply with a zero Hertz frequency span. Thus, when the spectrum analyzer sweeps, it measures the variation in amplitude of the 40 kHz current versus time.

B.1.1.2.1 Equipment Needed

- Power probe electronic tool or current probe,
- Low Frequency Spectrum Analyzer (e.g., HP 71110C)

B.1.1.2.2 Test Procedure

This test measures the ratio between a module's steady state power consumption and its peak transient power consumption. Therefore, it will be necessary to perform the Module Steady State Power Consumption Test first.

The setup for this test is shown in figure B-3. As in the steady state power measurement, the power probe electronic tool is connected to the power supply so that a module's load current can be measured. Alternatively, a current probe may be used. The current output of the probe is connected to the spectrum analyzer input.

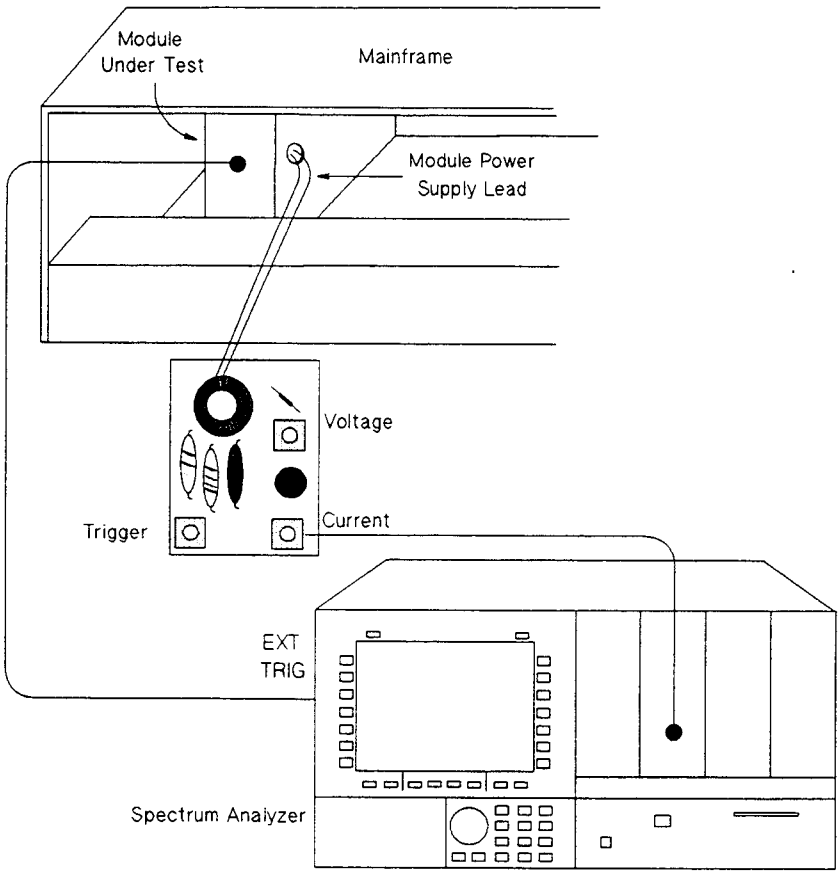


Figure B-3. Transient Power Consumption Test Setup

The spectrum analyzer is set to the frequency of the 40 kHz power supply, with a span of 0 Hz. Thus, as the spectrum analyzer sweeps, it will show the variations in the amplitude of the 40 kHz current versus time.

The spectrum analyzer must be set to trigger its sweep off some event that signals the change of state of the module. This will cause the spectrum analyzer to begin its sweep as the module begins to draw higher levels of current. For some modules, such a trigger output may be readily available. For others, it may be necessary to access signals internal to the module to get an appropriate trigger. For instance, a strobe line for latches that control mechanical switch drivers could be used if the switches' transient power consumption was to be measured. Or, if the module under test can be controlled over the GPIB bus, a short program could be written to trigger a single sweep of the spectrum analyzer and then change the state of the module.

Once the sweep has been taken, use the spectrum analyzer's marker functions to measure the ratio of the peak to steady state load current. Since the module's steady state power consumption is already known, calculating the transient power consumption is then an easy task. Suppose, for example, that the module under test consumes 18 watts steady state. The spectrum analyzer indicates a steady state current of 0.667 amps, with a peak current of 0.700 amps. The transient power consumption then is

$$P = 18W \times \frac{.700A}{.667A} = 18.9W$$

If the steady-state power consumption test described in the previous section is not performed, this technique can be used as an absolute module power consumption measurement. The absolute amplitude accuracy of the spectrum analyzer will probably need to be calibrated to ensure reasonable measurement accuracy. Even so, this power measurement technique does involve certain approximations. The spectrum analyzer measures only the amplitude of the 40 kHz component of the load current. Since the current is nominally a square wave, its spectrum will show a large number of high level harmonics of 40 kHz. However, for the purposes of measuring module power consumption, these harmonics can be ignored. This is because the power supply voltage is a relatively clean sine wave, with only small levels of harmonics present. We can calculate the power consumption by integrating the product of the voltage times the current over one cycle:

$$P = \frac{1}{\tau} \int_0^{\tau} V(t)\, I(t)\, dt$$

This can be expanded as

$$P = \frac{\omega_0}{2\pi} \int_0^{2\pi/\omega_0} V_0 \cos(\omega_0 t) \left[I_0 \cos(\omega_0 t) + I_1 \cos(2\omega_0 t) + I_2 \cos(3\omega_0 t) + \ldots \right] dt$$

Evaluating this integral shows that power is delivered only by the fundamental component of the current. The 120 kHz, 200 kHz, and higher harmonics of current deliver no power to the load. Thus, measuring the amplitude of the fundamental of the current is sufficient for calculating power consumption. This approximation has been tested experimentally and has been found to yield an error of less than 2% for typical modules.

B.1.2 Power Supply Regulation Tests

B.1.2.1 Module Load Current Sidebands Test

B.1.2.1.1 Equipment Needed

- MMS mainframe (e.g., HP 70001A)
- Current probe (e.g., Tektronix A6302)
- Low frequency spectrum analyzer (e.g., HP 71100C)

B.1.2.1.2 Test Procedure

The modulation load current sidebands test measures variations of the amplitude of the 40 kHz current drawn by the module from the mainframe power supply. This can be observed in the frequency domain by measuring the 40 kHz component of the module's load current on a spectrum analyzer. Variation in the amplitude of the load current will be seen as sidebands on the 40 kHz carrier. The maximum level of these sidebands, relative to the maximum allowed amplitude of the 40 kHz carrier, are shown in figure B-4.

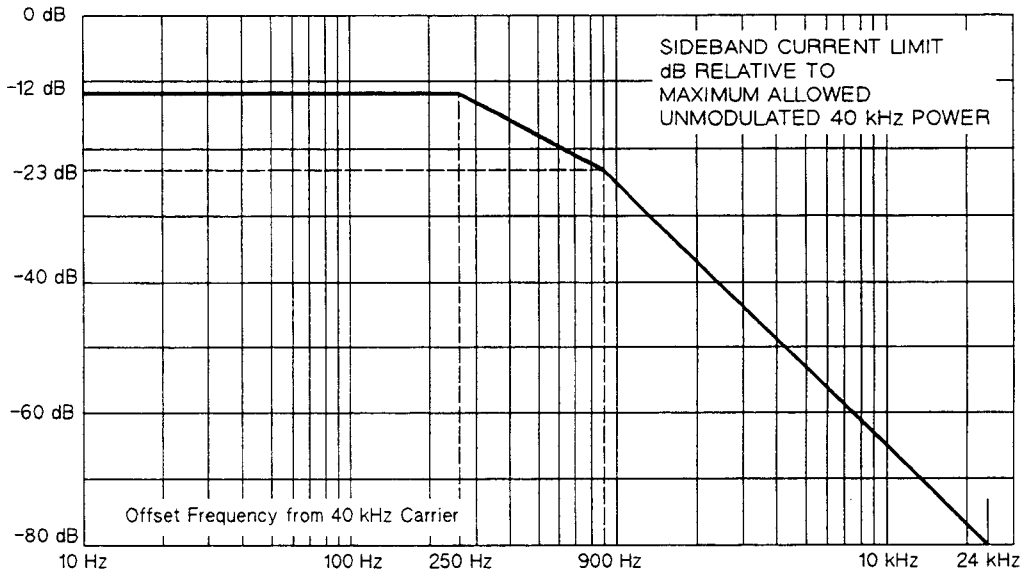


Figure B-4. Maximum Sideband Limits

In order to measure the current drawn by the module power supply, it will be necessary to gain access to the 40 kHz power bus. The easiest place to do this is at the module fuse.

The equipment setup for this test is shown in figure B-5. The module should be inserted into the mainframe. Clip the current probe around either AC-A or AC-B. Set the module to the state that will maximize the variation in its power supply current, and measure the sidebands of the 40 kHz carrier on the spectrum analyzer. It is important to note that the sideband limits in figure B-4 are expressed relative to the maximum unmodulated carrier. High levels of modulation will decrease the amplitude of the carrier, because energy is transferred from the carrier to the sidebands. Measuring sidebands relative to the carrier seen on-screen will therefore be inaccurate when the sideband levels are high. For this reason, it is necessary to measure the sideband levels in absolute units, rather than relative to the 40 kHz carrier. They should then be compared to the maximum 40 kHz current that the module under test is allowed to draw. The maximum 40 kHz component of a module's load current can be calculated from the equation

$$I = \text{Power}/27 \text{ volts}$$

where 27 volts is the nominal rms power supply voltage, and the power is the maximum allowed power consumption of the module under test.

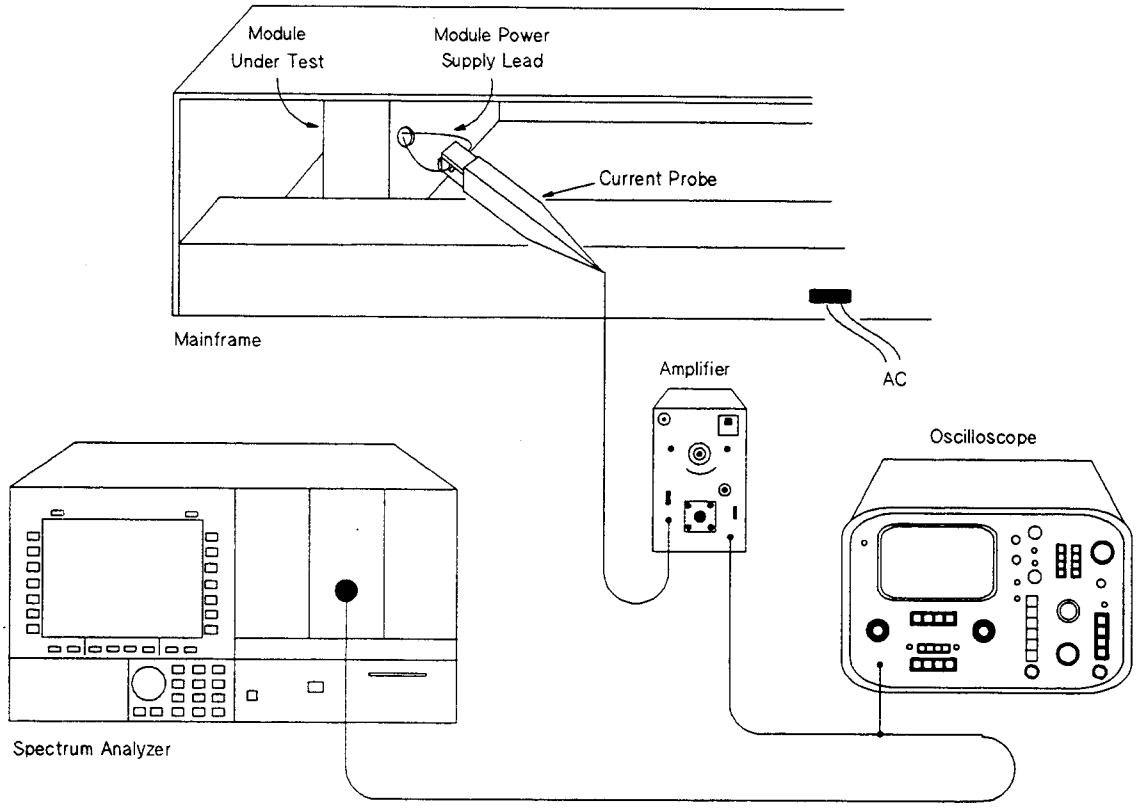


Figure B-5. Module Load Current Sidebands Test Setup

The distinction between the amplitude of the 40 kHz current and the maximum unmodulated current is important. Figure B-4 shows that it is necessary to be able to measure sideband levels 12 dB below the maximum allowed unmodulated current at offsets as low as 10 Hz. Using a spectrum analyzer with a 3 dB resolution bandwidth of 10 Hz, it is not possible to measure signals 12 dB below a carrier at this offset. However, as mentioned above, if the current is modulated with sidebands of this level, the amplitude of the carrier will be reduced. This will increase the dynamic range of the measurement, making it possible to measure the sidebands at the required levels.

B.1.2.2 Mainframe Power Supply Dynamic Voltage Accuracy

This test measures variations in a mainframe's power supply voltage caused by variations in modules' load current. Since the mainframe power supply has a nonzero output impedance, variations in the amplitude of the current drawn by modules will cause corresponding variations in the mainframe power supply output voltage. If the variations are periodic, these will appear as sidebands on the 40 kHz power supply voltage. This test draws a periodically varying current from the mainframe and measures the amplitude of the resulting sidebands.

B.1.2.2.1 Equipment Needed

- Average detector ET, (construction details for this ET are given in section B.1.2.3).
- Nonlinear load ET, (construction details for this ET are given in section B.3.1.2.3).
- Network analyzer, 10 Hz to 10 kHz (e.g., HP 3577)
- Current probe, DC to 10 kHz (e.g., Tektronix A6302)
- Oscilloscope
- Electronic load (e.g., Transistor Devices DLP50-60-1000A Dynaload)
- 220 μF, 25 V electrolytic capacitor
- 1 ohm, 1/4 watt resistor
- Electronic load modulation circuit (described below)
  - Optoisolator (e.g., General Instrument CNY65)
  - 470 μF, 10 V electrolytic capacitor
  - 2 100 ohm, 1/4 watt resistors
  - 1000 ohm, 1/4 watt resistor

B.1.2.2.2 Test Procedure

This test measures the impedance of the mainframe power supply. A rectifier is used to convert the 40 kHz power supply voltage to DC. An electronic load is connected to the rectifier's output. The amplitude of the load current is modulated by connecting the output of a network analyzer to the electronic load's modulation input. The average detector ET is used to detect the amount of ripple on the power supply voltage. A current probe is used to measure the ripple current. By using the network analyzer to measure the ratio of voltage to current, it is possible to get a direct measurement of the impedance of the mainframe power supply as a function of the modulation frequency.

Set up the equipment as shown in figure B-6. The nonlinear load ET should be plugged into the slot that is electrically farthest from the power supply. This will guarantee a worst case measurement, since the impedance of the entire power distribution bus will be measured. The demodulator ET should be plugged into the slot that is electrically the closest to the slot that the nonlinear load is in.

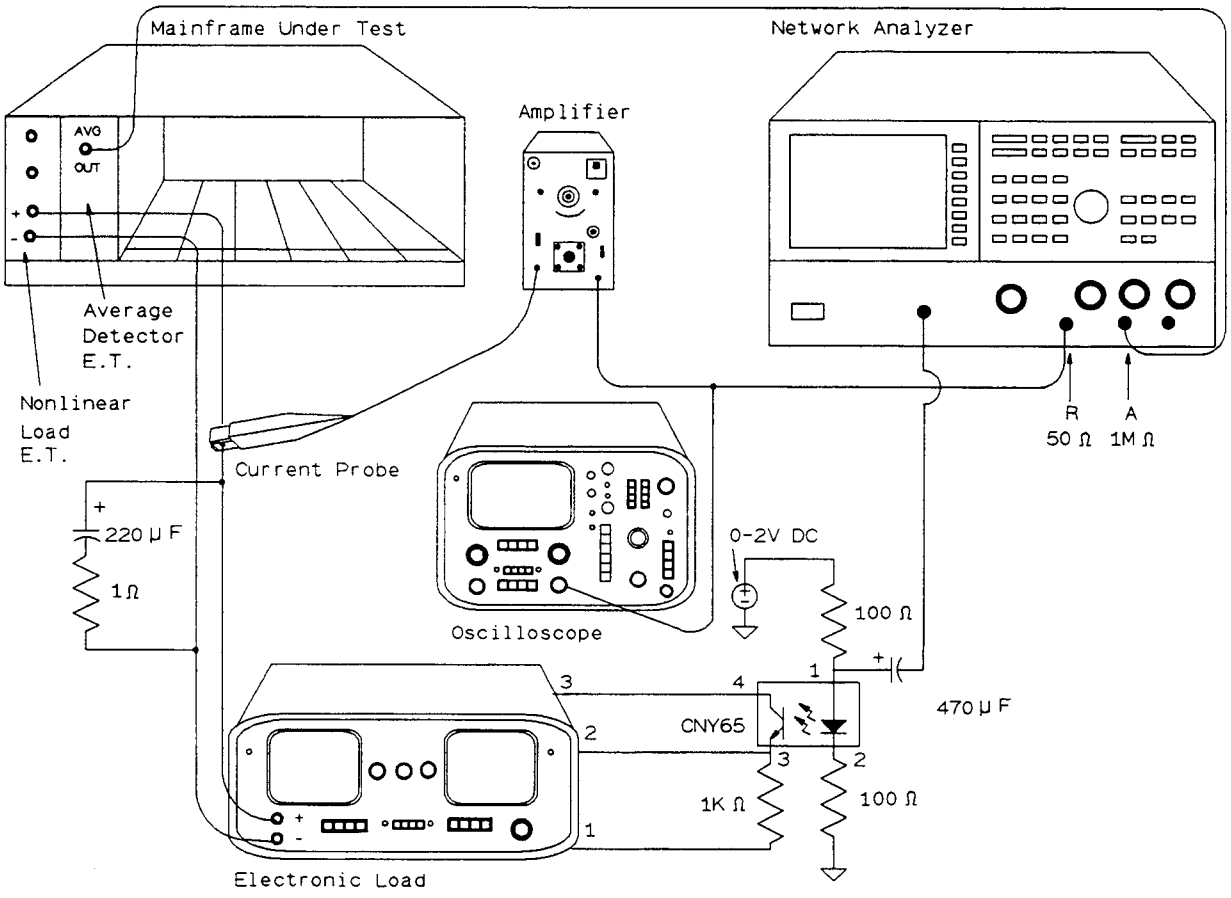


Figure B-6. Mainframe Load Current Modulation Test Setup

The nonlinear load ET converts the 40 kHz power supply into a DC voltage. The output of the nonlinear load ET is connected to the electronic load. Since the output of the nonlinear load is differential and balanced with respect to ground, the electronic load's input terminals must float with respect to ground. This means that the modulation signal applied to the electronic load's modulation input terminals must float with respect to ground also. The interface circuit shown in figure B-6 between the network analyzer and the electronic load will accomplish this. An optoisolator is used to transform the ground-referenced output of the network analyzer into a floating signal.

The "A" channel input of the network analyzer is connected to the output of the average detector ET. This ET rectifies and filters the 40 kHz power supply voltage, producing a video output proportional to the average value of the 40 kHz waveform. The "R" channel input is connected to the output of the current probe, which measures the current at the nonlinear load ET output.

It may be necessary to connect a capacitor across the output terminals of the electronic load. If the capacitor is not present, the load will see the relatively high output impedance of the nonlinear load ET and may oscillate. It has been found that a 220 μF aluminum electrolytic capacitor in series with a one ohm resistor across the output terminals of the Transistor Devices load is sufficient to ensure stability. Note that capacitor should be placed between the current probe and the electronic load, rather than between the current probe and the ET. Improper placement will cause an incorrect current measurement.

To configure the system for the measurement, adjust the electronic load so that the nominal load current is half of the maximum rated current of the mainframe. Set the output level of the network analyzer to the desired amplitude. Connect the output of the current probe to an oscilloscope, and to the network analyzer "A" input. Adjust the gain of the current probe amplifier as high as possible, while making sure that the waveform on the oscilloscope is not distorted.

Sweep the frequency of the network analyzer from 10 Hz to 10 kHz. A display of the ratio A/R will display the impedance of the mainframe as a function of modulation frequency. It will be necessary to account for the gain of the current probe amplifier and the gain of the average detector in order to calculate the absolute magnitude of the impedance measured. For instance, suppose that at a modulation frequency of 5 kHz, we measure 5 mV at the average detector output, and 100 μV at the current probe output with the current probe scale set to 2A = 10 mV. Since the average detector ET has a gain of 1/2, we would calculate the impedance as follows:

$$I = 100\,\mu V \times (2A/10mV) = 20\,mA$$

$$V = 5\,mV \times 2 = 10\,mV$$

$$Z = V/I = 10\,mV/20\,mA = 0.5\,\Omega$$

The impedance measured as a function of modulation frequency should be less than the limits shown in figure B-7.

The maximum allowable impedance of the mainframe can be calculated from the mainframe specification for dynamic voltage accuracy (table 3-1) and the module specification for module load current variation (figure 3-4). The mainframe's output voltage must vary by less than the dynamic voltage accuracy specification when subjected to variations in module load current. The maximum mainframe impedance versus the rate of load current variation is shown in figure B-7. Z_0 for a given mainframe can be calculated from the equation

$$Z_0 = \frac{2 \times \Delta \times (24.3)^2}{P_{max}}$$

where P_{max} is the mainframe's maximum specified output power, and Δ is the maximum dynamic voltage accuracy of the mainframe. For example, for a 200 watt mainframe with a dynamic voltage accuracy specification of ± 1%,

$$Z_0 = \frac{2 \times (0.01) \times (24.3)^2}{200} = 59\,m\Omega$$

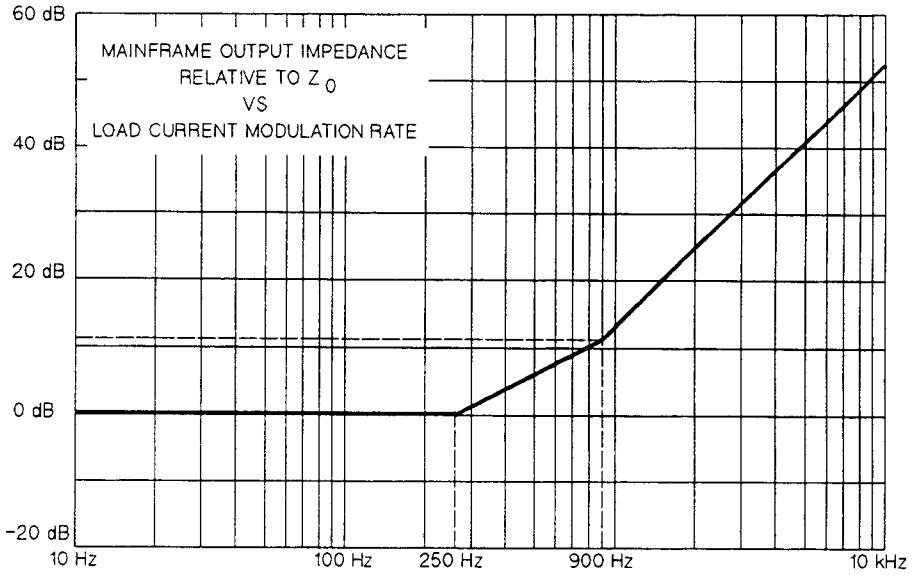


Figure B-7. Mainframe Output Impedance

B.1.2.3 Construction Procedure for the Average Detector ET

This ET is used to measure the average value of the 40 kHz power supply voltage. The circuitry rectifies the 40 kHz voltage and low pass filters the rectified waveform, producing a DC output equal to the one-half the average amplitude of the power supply voltage.

A schematic of the ET is shown in figure B-8. The ET should be built into a one slot width module. Note that the common node of the circuitry is not connected to chassis ground, but is rather tied only to the 40 kHz return on the backplane interface connector.

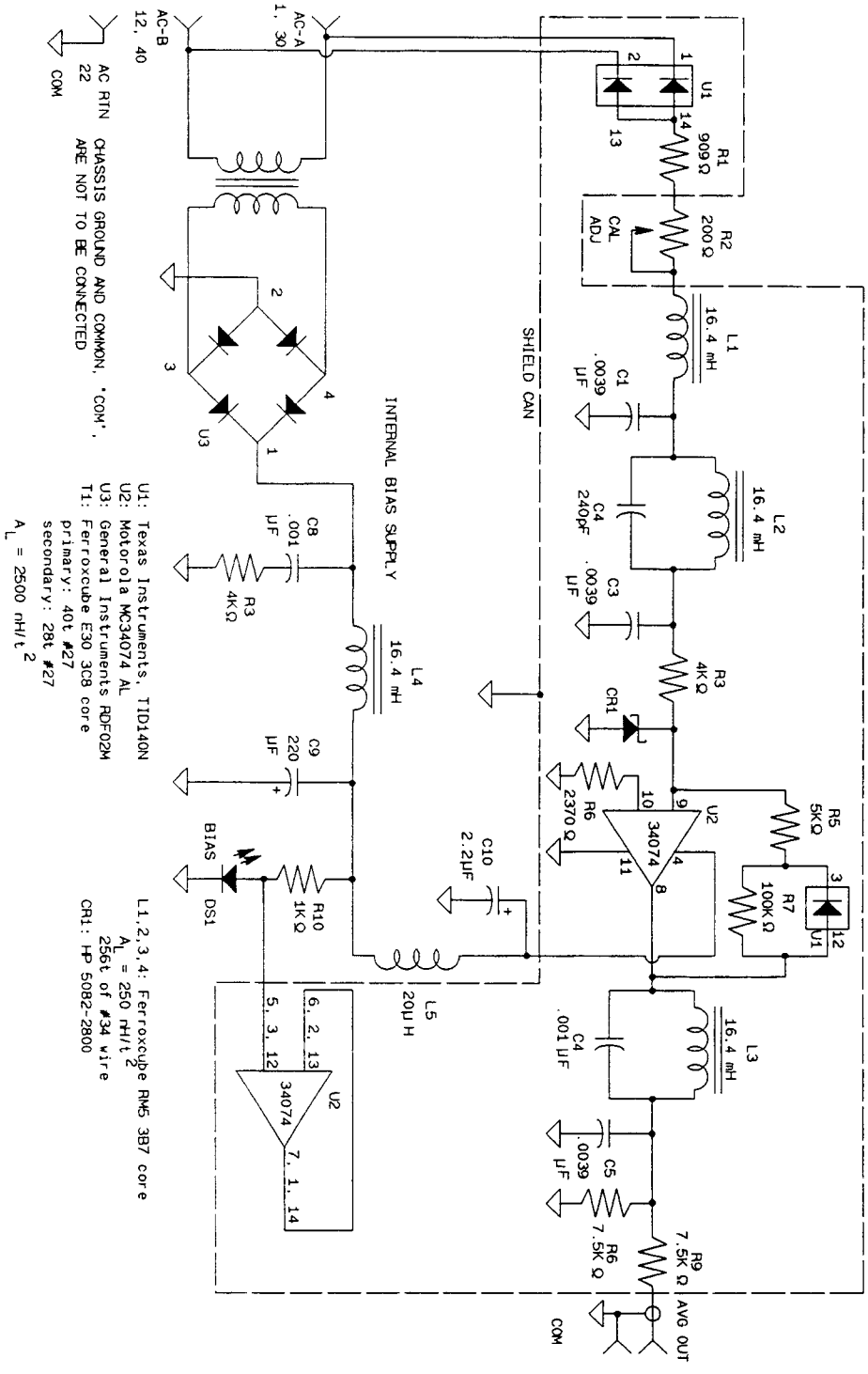


Figure B-8. Average Detector ET Schematic

To calibrate the ET, insert it into an empty mainframe. Since the amplitude of the mainframe's power supply is specified to be accurate within two percent, we can use this to calibrate the gain of the

average detector. Adjust the potentiometer until the output of the ET is 12.15 volts. Since the nominal average power supply voltage is 24.3 volts, the average detector has a gain of 0.5. This gain must be taken into account when using the ET.

The accuracy of this calibration method should be sufficient for the tests described in appendix B.2. If a more accurate calibration of the average detector ET is desired, it may be calibrated using the test procedure described in appendix B.1. That appendix describes a technique for making accurate measurements of mainframe power supply average voltage, which may then be used to calibrate the ET.

B.2 Magnetic Field Emissions and Susceptibility

B.2.1 Emissions from Modules and Mainframes

The measurement of magnetic field emissions is a two step process. The first step is to develop the probes necessary for the test. The second is to perform the actual measurement.

When developing or procuring the probes for the test, the following factors should be kept in mind:

1. The probes must have sufficient sensitivity to be able to make the measurements to the desired limits.
2. The probes must be able to make the measurements over the frequency range of interest. In general, there is a trade off between sensitivity and high frequency response. Because of this, it may be necessary to use multiple probes to cover the entire frequency range.
3. The probes must be small enough. The output of a magnetic field probe is typically proportional to the average magnetic field through its measurement aperture. If the magnetic field varies rapidly over small distances, the probe's output will show the average value over its measurement aperture, rather than the peak. This will result in lower readings. Therefore, the size of the probe should be as small as possible. Unfortunately, a small probe is in general less sensitive than a larger one. The maximum allowable size of the probe is specified in rule 8.1.1.1.1-1 for modules, and rule 8.2.1.1.1-1 for mainframes.
4. The probes must have a known sensitivity and frequency response. If appropriate probes can be purchased with a specified sensitivity across the measurement band, this is simple. Otherwise, it will be necessary to find the sensitivity of the probe. This can be measured by immersing the probe in a uniform plane wave of known strength, and measuring the output. At low frequencies, it may be possible to calculate the sensitivity of some probes with good accuracy through the laws of electromagnetics. At higher frequencies, this may be more difficult.
5. The design of the probe should be such that the measurement aperture can be placed close to the module surface. The strength of the magnetic fields emitted by modules typically falls off very rapidly with distance. Unless the measurement is made close to the module surface, the results will be inaccurate.
6. The probe should be designed to be insensitive to E-fields. Since the emissions of modules are predominantly magnetic, superior E-field rejection is not necessary. Nevertheless, probes that offer some degree of E-field rejection should yield more repeatable and more accurate results. Balancing or shielding of the probes may be used to achieve this.

Given these constraints, there are several options. HP 11940A and 11941A probes may be used. Unfortunately, these probes are physically large. This makes it difficult to fit them into a mainframe along with a module in order to make the measurement. For one slot width modules there should be enough room to do this. The EMCO #7405 Near Field Probe Set may also be usable. A module designer could also develop his own probes.

B.2.1.1 Measurement

B.2.1.1.1 Equipment Needed

- 10 Hz to 1 GHz magnetic field probes,
- 10 Hz to 1 GHz preamplifier,
- 10 Hz to 1 GHz spectrum analyzer (e.g., HP 71100C).

If a module is to be tested, it should be placed alone in a mainframe. If other modules need to be used to operate the module for this test, they should be in a second mainframe with appropriate connections running between the modules. The module under test should be placed so that its MSIB connector is in the fifth slot from the left of the MMS mainframe, if possible.

If a mainframe is to be tested, it should contain no modules.

Using the appropriate probe for the frequency range being tested, move the probe over the surface of the module or mainframe. Where high levels of emissions are found, rotate the probe until the maximum reading is recorded. The probe should be moved over both the left and right sides of the module or mainframe carefully, paying particular attention to holes and seams. The level of emissions recorded must not exceed the limits shown in figure B-9.

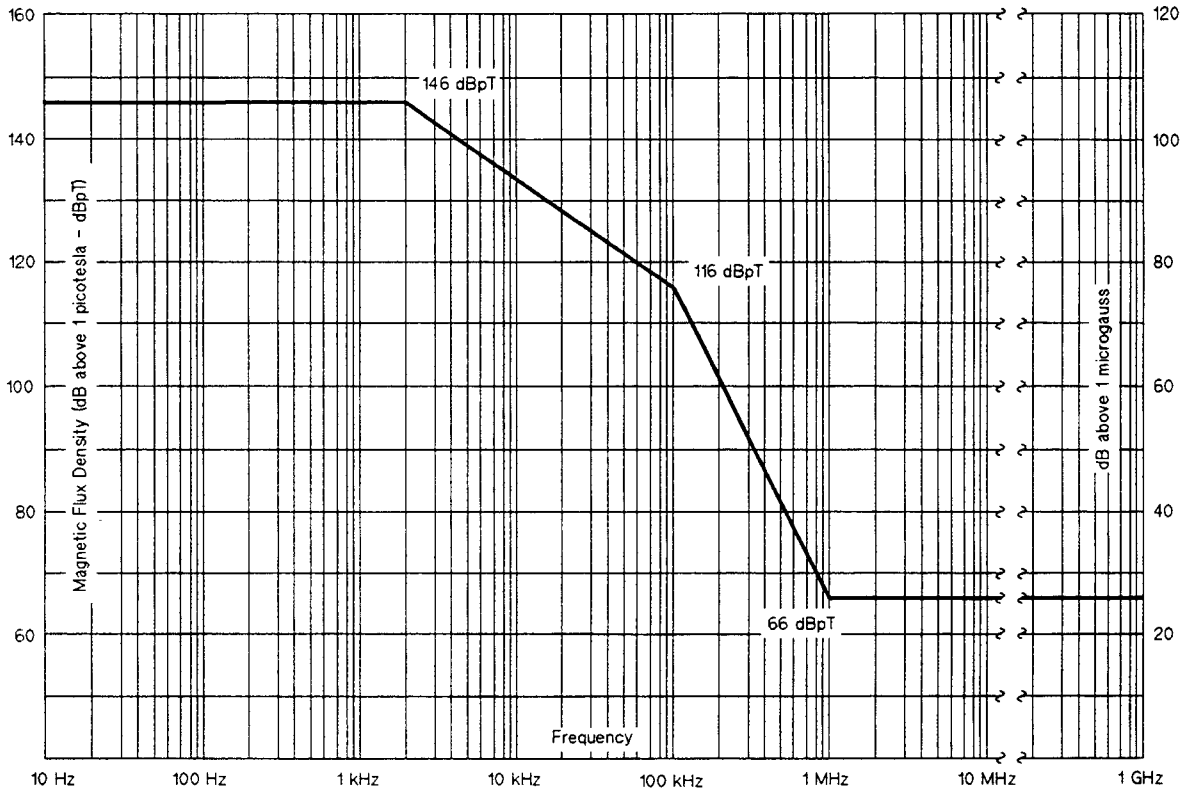


Figure B-9. Close-field Magnetic Emission Limits

Emissions are specified for the left side and right side of the module only. Emissions are not specified for the top, bottom, front, or rear module surfaces.

B.2.2 Susceptibility of Modules and Mainframes

The measurement of magnetic field susceptibility is a two step process. The first step is to develop the probes necessary for the test. The second step is to perform the actual measurement.

When developing or procuring the probes for the test, the following factors should be kept in mind:

1. The probes must be able to generate sufficient field strength to be able to test susceptibility to the desired limits.
2. The probes must work over the frequency range of interest. In general, there is a trade off between sensitivity and high frequency response. Because of this, it may be necessary to use multiple probes to cover the entire frequency range.
3. The probes must be large enough. The magnetic field generated by a probe falls off rapidly with distance. In general, the smaller the probe, the more rapidly the field strength will decay. For this reason, probes with extremely small apertures will not generate fields that extend far into the module under test. The minimum allowable size of the probe is specified in rule 8.1.1.2.1-1 for modules, and rule 8.2.1.2.1-1 for mainframes.

4. The probes must have generate a known field strength over the frequency band of interest. This can be done by measuring the field strength generated with a second, calibrated probe. At low frequencies, it may be possible to calculate the field strength generated by simple probes with good accuracy using the laws of electromagnetics. At higher frequencies, this may be more difficult.
5. The design of the probe should be such that the measurement aperture can be placed close to the module surface. The strength of the magnetic fields generated by probes typically falls off rapidly with distance. Unless the measurement is made close to the module surface, the results will be inaccurate.
6. The probe should be designed to be generate minimal E-fields. It is expected that most modules will not be overly sensitive to electric field emissions. Nevertheless, probes that offer some degree of E-field rejection should yield more repeatable and more accurate results.

Given these constraints, there are several options. HP 11940A and 11941A probes may be used. Unfortunately, these probes are physically large. This makes it difficult to fit them into a mainframe along with a module in order to make the measurement. For one slot width modules there should be enough room to do this. The EMCO #7405 Near Field Probe Set may also be usable. Note that none of these probes specify their sensitivity when they are used to produce magnetic fields. Finally, the module designer could develop his own probes.

B.2.2.1 Measurement

B.2.2.1.1 Equipment Needed

- 10 Hz to 1 GHz magnetic field probes,
- 10 Hz to 1 GHz preamplifier,
- 10 Hz to 1 GHz source.

To perform the close-field magnetic susceptibility test on a module, the module must be in a mainframe alone. If other modules need to be used to operate the module for this test, they should be in a second mainframe with appropriate connections running between the modules. The module under test should be placed so that its backplane interface connector is in the fifth slot from the left of the MMS mainframe, if possible.

If a mainframe is to be tested, it should contain no modules.

Set the output of the amplifier to a level sufficient to generate a field strength 10 dB to 20 dB higher than the specification limit. Set the frequency range of the signal source to the appropriate range for the probe being used.

Using the appropriate probe for the frequency range being tested, move the probe over the surface of the module or mainframe. Simultaneously, monitor the performance of the module or mainframe under test. At locations where performance degradation is found, adjust the power output of the amplifier until performance is degraded to the limits of the products specification. This magnetic field strength must not be less than the susceptibility limits defined in figure B-10.

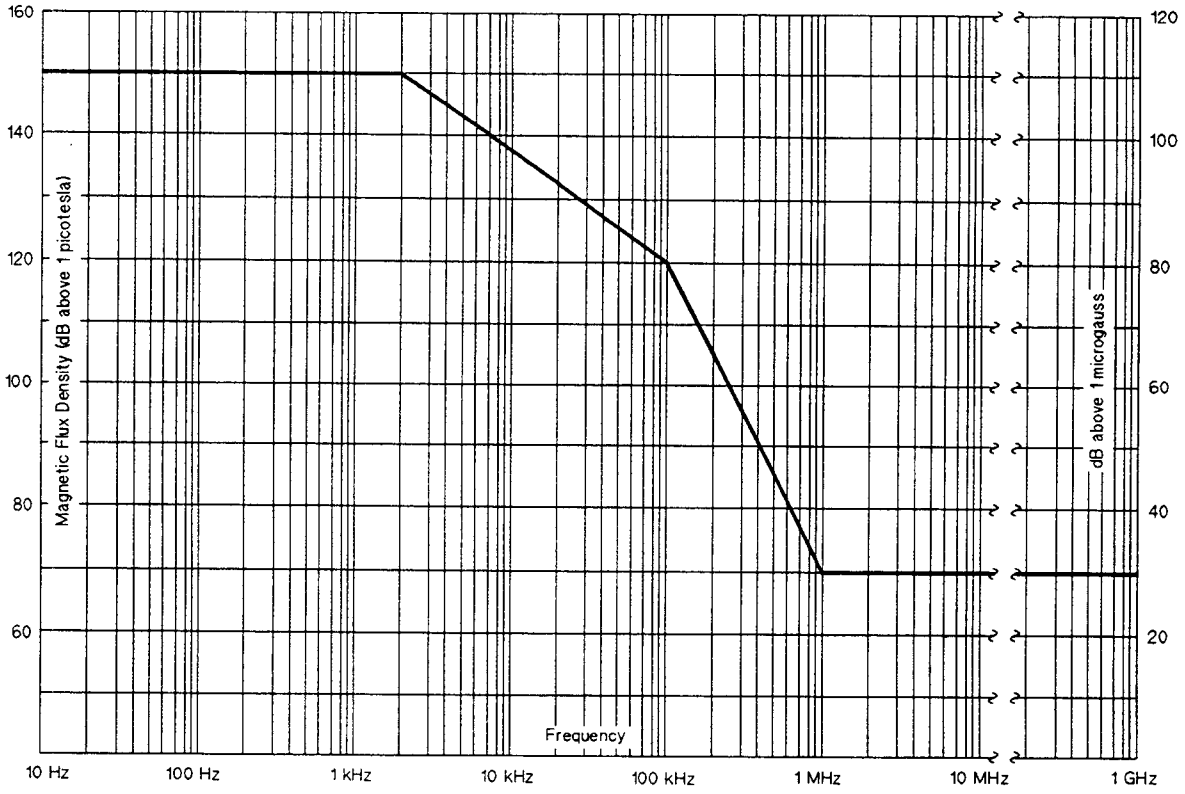


Figure B-10. Close-field Magnetic Susceptibility Limits

Susceptibility is specified for the left side and right side of the module only. Susceptibility is not specified for the top, bottom, front, or rear module surfaces.

B.3 Power Bus Conducted Emissions and Susceptibility

B.3.1 Mainframe Power Bus Conducted Emissions and Susceptibility

B.3.1.1 Mainframe Power Bus Conducted Emissions

The mainframe power bus conducted emissions tests consists of three parts. These measure different aspects of the power bus's performance. These tests measure:

1. Harmonics of the 40 kHz power supply waveform
2. Nonharmonic spurious signals
3. Ripple on the 40 kHz power supply waveform

The first two tests are described in this section. The third test, which measures power supply ripple, is described in the section B.1.2.2.

B.3.1.1.1 Equipment Needed

The following equipment will be necessary for these tests:

- Spectrum analyzer, 100 Hz to 200 MHz response (e.g., HP 71100C),
- Mainframe Emissions Electronic Tool (ET); construction details for this ET are described in section B.3.1.1.4.

B.3.1.1.2 Power Supply Harmonics Test

The mainframe supplies power to modules in the form of a 40 kHz AC voltage waveform. Harmonics of this voltage are measurable well into the megahertz region. The harmonic content of the signal is measured with the mainframe emissions ET. The construction of this ET is described in section B.3.1.1.4. The ET provides access to both the AC-A and AC-B phases of the power supply. The harmonic content of both phases can then be measured with a spectrum analyzer. Since the power supply voltage is nominally 24.3 volts AC average across the phases, it is necessary to attenuate this signal before it is connected to the spectrum analyzer used to measure the harmonics. The ET provides 29.6 dB of attenuation.

To make the measurement, the ET is inserted into the mainframe under test. In order to ensure consistency of results, the slot into which the ET is inserted needs to be specified. For this test, the ET should be inserted into the slot immediately to the left of center in the mainframe. For instance, in an eight slot mainframe, the test is performed in the fourth slot from the left. No other modules should be in the mainframe when the test is performed.

The voltage at the AC-A and AC-B outputs of the ET are measured on the spectrum analyzer. The harmonic levels, relative to the fundamental, must not exceed the limits in figure 8-8.

B.3.1.1.3 Non-Harmonic Spurious Test

It is also possible to have signals present on the power supply bus which are not harmonically related to the power supply fundamental. Experience has shown that these signals typically appear on AC-A and AC-B common mode with respect to ground. This test therefore measures the level of non-harmonic common mode signals on the power bus.

The mainframe emissions ET, described in section B.3.1.1.4, is used to make this measurement. As in the power supply harmonics measurement, the ET is inserted into the mainframe slot immediately to the left of center. The common mode output of the ET is measured on the spectrum analyzer. Note that since the common mode output has 29.6 dB of attenuation, 29.6 dB must be added to the measurement results to calculate the correct signal level.

It will be possible to observe many harmonics of the power supply voltage during this test. Since this test is only for non-harmonic signals, these should be ignored. The specification limits for non-harmonic spurious are shown in figure B-11.

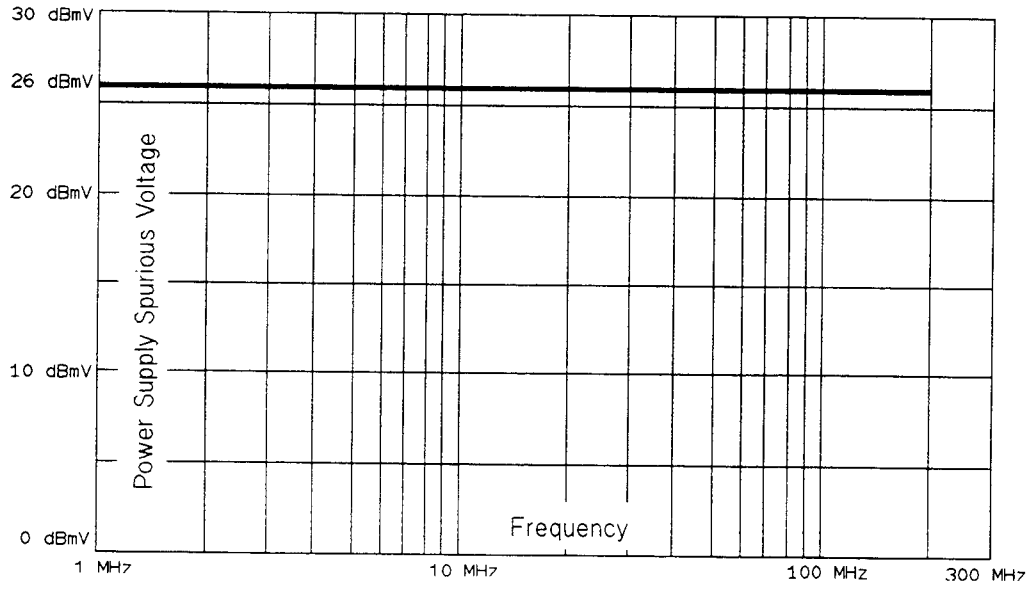


Figure B-11. Mainframe Common Mode Spurious

B.3.1.1.4 Construction Procedure for the Mainframe Emissions ET

The mainframe emissions ET is used to measure voltage disturbances on the mainframe power bus. It provides attenuated outputs for both phases of the power bus, as well as a common mode output.

A schematic of the ET is shown in figure B-12. The ET should be built in a one slot width module frame. Since the ET will be used at frequencies as high as 200 MHz, good high-frequency construction techniques should be used.

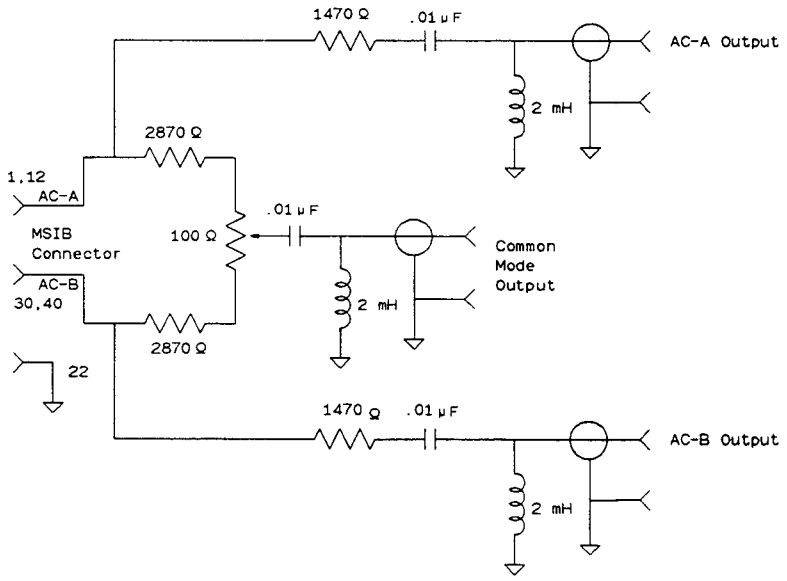


Figure B-12. Mainframe Emissions ET

A potentiometer is provided to balance the common mode output. This is adjusted by inserting the ET into a mainframe and connecting the ET's common mode output to a 50 ohm oscilloscope. Adjust the potentiometer until the minimum signal level is displayed on the oscilloscope.

This ET is designed to attenuate the signals on the power bus to prevent overloading the spectrum analyzer used to make the measurements. Because of this, the user must add a calibration factor to the measured output. This correction factor is 29.6 dB for all outputs.

B.3.1.2 Mainframe Power Bus Conducted Susceptibility

The quality of the 40 kHz power signal provided by a mainframe is influenced by the characteristics of the modules that use that power. Because the degradation caused by one module can affect the performance of another module, it is necessary to specify the susceptibility of the mainframe to this type of performance degradation. These tests measure:

1. Susceptibility to harmonics of modules' non-sinusoidal load current
2. Susceptibility to non-harmonic spurious current
3. Susceptibility to load current modulation

The first two tests are described in this section. The third test, which measures ripple induced on the power supply by varying module loads, is described in section B.1.2.2.

B.3.1.2.1 Mainframe Power Supply Harmonic Susceptibility

B.3.1.2.1.1 Equipment Needed

- Nonlinear Load ET; construction details for this ET are described in section B.3.1.2.3,
- Mainframe Emissions ET; construction details for this ET are described in the section B.3.1.1.4,
- Current Probe: DC-10 MHz Response (e.g., Tektronix A6302)
- Electronic load (e.g., Transistor Devices DLP50-60-1000A Dynaload)
- Spectrum analyzer, 100 Hz to 10 MHz (e.g., HP 71100C)

B.3.1.2.1.2 Test Procedure

Ideally, the voltage present on the mainframe power bus is a perfect 40 kHz sine wave. However, harmonics of this sine wave are also present. The level of these harmonics is affected by the modules present in the mainframe. This is because the load current drawn from the power supply is highly nonlinear, and therefore the current drawn by modules contains significant current at harmonics of the 40 kHz fundamental. Because the mainframe has a non-zero output impedance, these harmonics of the fundamental current can generate voltages on the bus at harmonics of the fundamental voltage.

This test will measure the large-signal impedance of the mainframe's power bus at harmonics of the power supply frequency. Since the harmonic content of modules' load current is specified, a proper impedance specification will guarantee that the worst-case levels of voltage harmonics appearing on the bus fall within acceptable limits.

The test is performed by placing a well-defined non-linear load on the power supply bus. The current drawn by the load is measured, as well as the voltage induced on the bus by the load. These measurements are made at several harmonics of the 40 kHz fundamental. Based on these measurements, the impedance of the bus is calculated.

The non-linear load ET is designed to produce a load current waveform that closely approximates an ideal square wave. Fast recovery diodes are used in the rectifier to minimize spikes generated during switching. A large filter inductor is used to reduce the amount of ripple in the rectified load current. An electronic load is connected to the output of the ET, and the load current is adjusted to the maximum specified current for the mainframe.

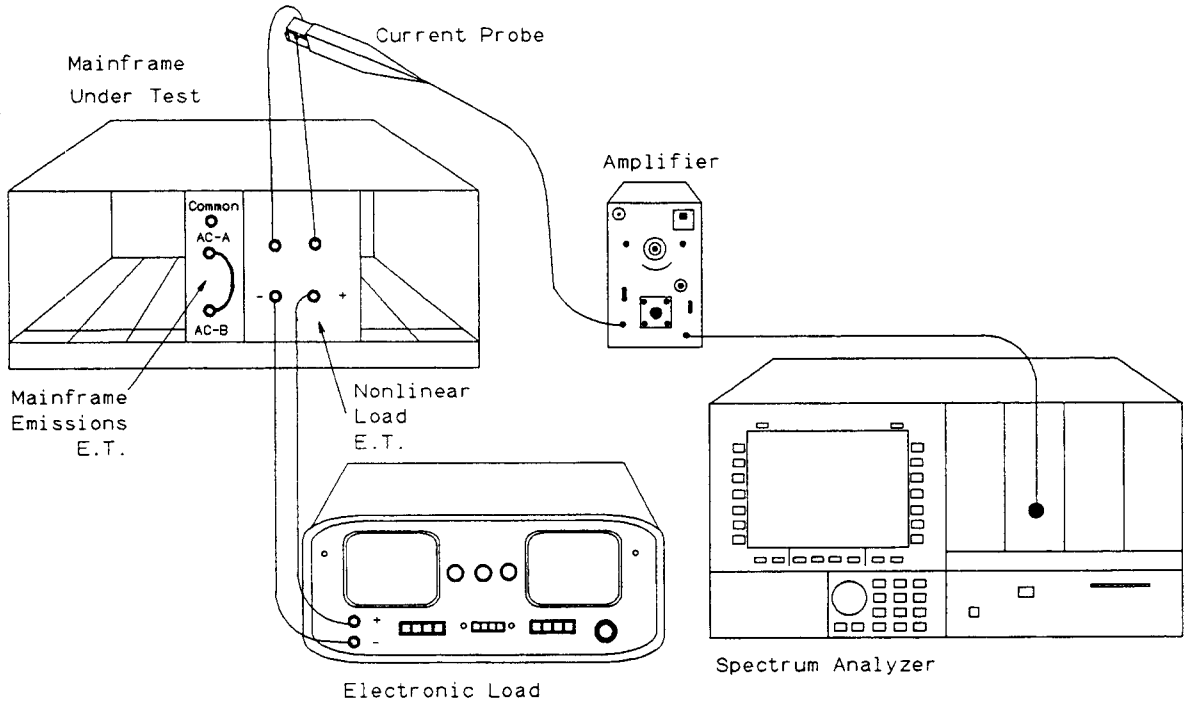


Figure B-13. Mainframe Power Supply Harmonic Susceptibility Test

The equipment setup for this test is shown in figure B-13. The mainframe emissions ET should be inserted into the mainframe. In order to ensure consistency of results, the slot into which the ET is inserted must be specified. For this test, the mainframe emissions ET should be inserted into the slot immediately to the left of center in the mainframe. For instance, in an eight slot mainframe, the ET would be inserted into the fourth slot from the left. The non-linear load ET should be inserted in the slot immediately to the right of this.

The output of the non-linear load ET is connected to the electronic load. The current drawn by the electronic load is adjusted so that the mainframe is supplying its maximum rated power to the load. For example, with a 200 watt mainframe, the load current would be set to $\frac{200 \text{ watts}}{24.3 \text{ volts}} = 8.23 \text{ Amps}$

The next step is to measure the different frequency components of the current drawn from the mainframe. The current probe is clipped around the lead that is routed through the rear panel of the nonlinear load. The output of the current probe amplifier should be monitored on a 50 ohm oscilloscope, and the amplifier gain should be adjusted as high as possible without causing distortion of the waveform. The output should then be connected to the spectrum analyzer. The spectrum analyzer will show a current spectrum rich in high order harmonics. The levels of these harmonics should be recorded at as many frequencies as is necessary to guarantee compliance with the specification.

The mainframe's power supply voltage is next measured at these same frequencies. The best way to measure the differential voltage between AC-A and AC-B is to connect a short between the AC-A and AC-B outputs of the mainframe emissions ET. By clipping the current probe around the shorting wire, it is possible to measure a current that is proportional to the voltage between the phases. The output of the probe amplifier should again be monitored on the oscilloscope and the amplifier gain should be set to the highest possible level that does not distort the waveform. Next, connect the probe amplifier

output to the spectrum analyzer. Measure the amplitudes of the harmonics at the same frequencies at which data was recorded before. Then calculate the power supply voltage at each of these frequencies from the recorded data. The differential voltage can be calculated by multiplying the measured current by 2940 ohms, the internal impedance of the ET.

From this data it is possible to calculate the impedance of the mainframe power supply at the frequencies for which data was recorded. Divide the measured voltage by the measured current at each frequency. The result will give the power supply's differential large signal impedance at that frequency. This data is checked against the specification limits in figure B-14.

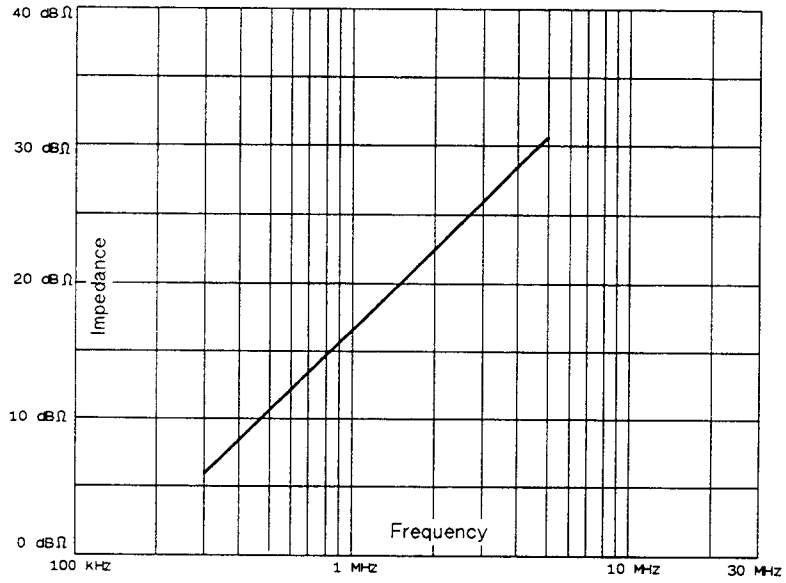


Figure B-14. Mainframe Harmonic Impedance

B.3.1.2.2 Mainframe Power Supply Non-Harmonic Susceptibility

B.3.1.2.2.1 Equipment Needed

- Mainframe Emissions ET (construction details for this ET are described in section B.3.1.1.4,
- Current Injection ET (construction details for this ET are described in section B.3.1.2.4,
- Low Frequency Current Probe: DC-50 MHz Response (e.g., Tektronix A6302)
- High Frequency Current Probe (construction details for this probe are described in section B.3.1.2.3)
- Network Analyzer, 100 Hz to 200 MHz (e.g., HP 3577)

B.3.1.2.2.2 Test Procedure

The purpose of this test is to measure the susceptibility of the mainframe power supply to spurious power supply currents generated in modules. Because the impedance of the mainframe power supply is non-zero, these spurious currents cause corresponding spurious voltages to appear on the power supply bus. Since the magnitude of modules' spurious current emissions is specified, a proper mainframe impedance specification will insure that the worst-case spurious mainframe power supply voltages fall within acceptable limits.

Experience has shown that these spurious currents are primarily common mode on AC-A and AC-B. For this reason, the test measures only the common mode power supply impedance.

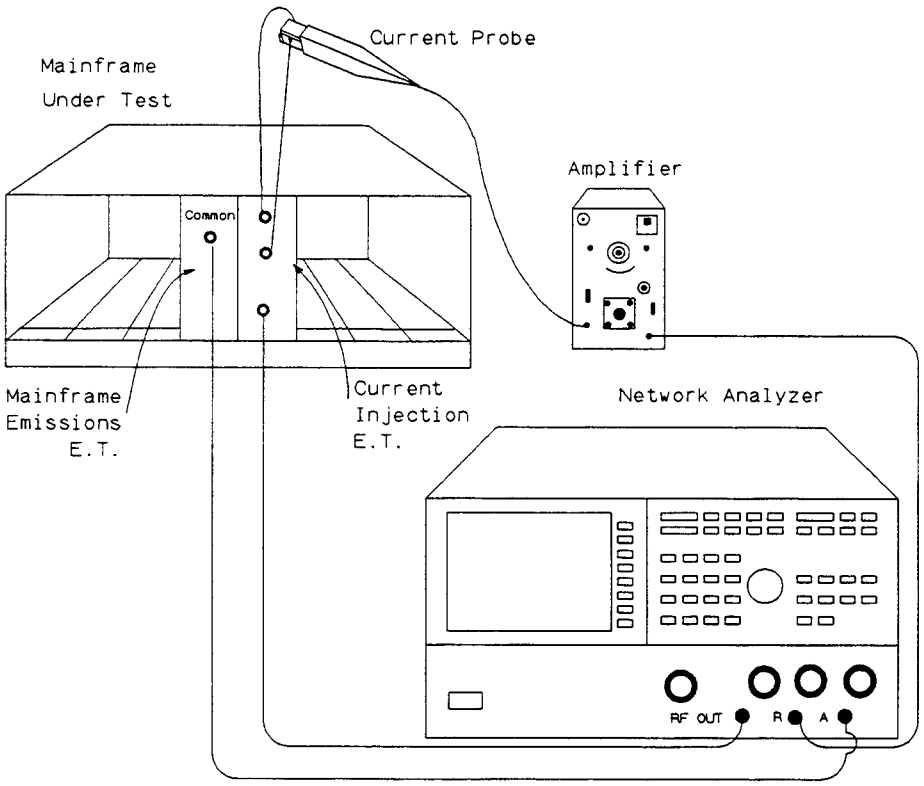


Figure B-15. Mainframe Power Bus Non-Harmonic Susceptibility Test

The equipment setup for this test is shown in figure B-15. The mainframe emissions ET should be inserted into the mainframe. In order to insure consistency of results, the slot into which the ET is inserted must be specified. For this test, the ET should be inserted into the slot immediately to the left of center in the mainframe. For instance, in an eight slot mainframe, the ET would be inserted into the fourth slot from the left. The current injection ET should be inserted into the slot immediately to the right of this.

The output of the network analyzer is connected to the source input of the current injection ET. The common mode output of the mainframe emissions ET is connected to the channel A input. The current probe is clipped around the wire loop which is routed through the front panel of the current emissions ET. The appropriate probe should be used for the frequency range being tested: the low frequency current probe should be used up to 50 MHz, and the high frequency current probe should be used between 50 MHz and 200 MHz. The output of the current probe is connected to the channel R

input of the network analyzer. By displaying an A/R ratio on the spectrum analyzer, it is possible to perform a direct impedance measurement. A calibration factor will need to be calculated for the current probe sensitivity and the attenuation of the mainframe emissions ET's common mode output. The impedance measured should be below the limits of figure B-16.

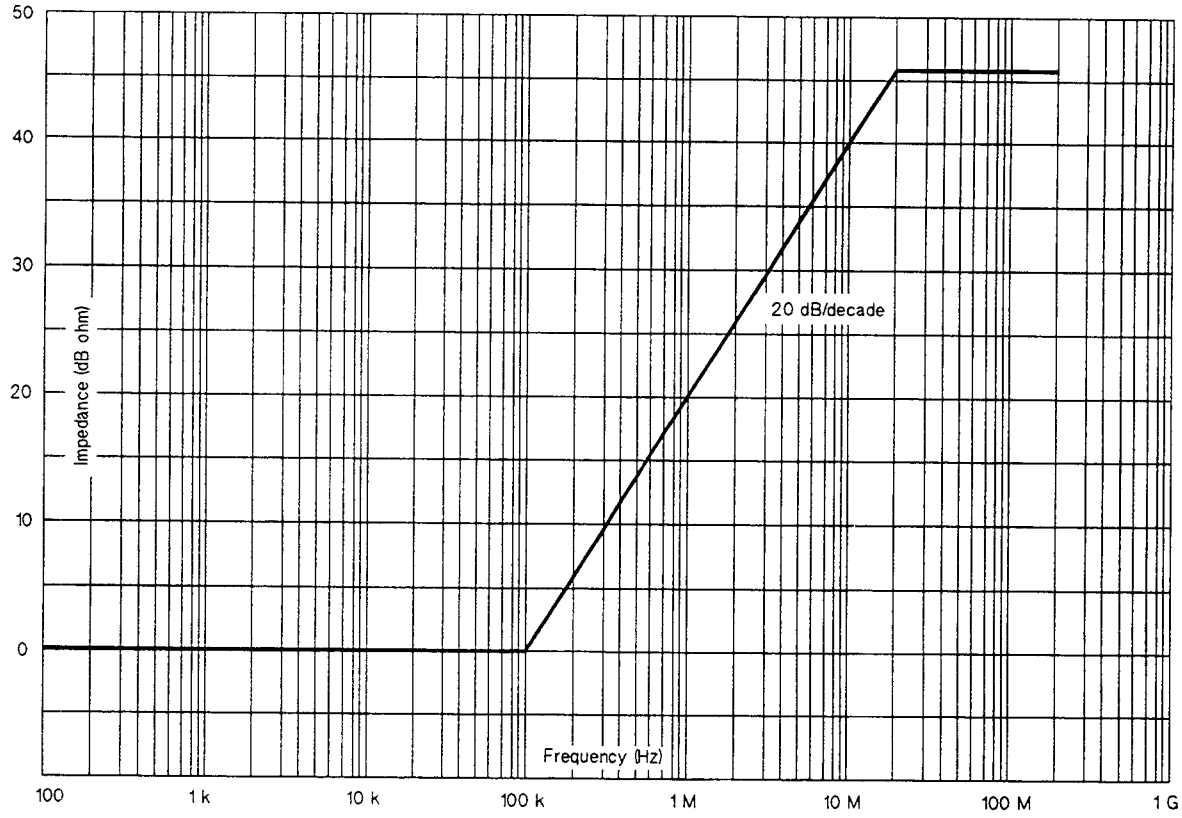


Figure B-16. Mainframe Common Mode Output Impedance

B.3.1.2.3 Construction Procedure for the Nonlinear Load ET

The nonlinear load ET is used to place a controlled and well-defined load on the mainframe power supply. The load current drawn from the mainframe by this ET is a good approximation of a square wave.

The ET is built in a two slot width module. A schematic for the ET is shown in figure B-17. The diodes rectify the 40 kHz power supply waveform, and the transformers low pass filter the diode's rectified output. Because of the large currents flowing through the rectifiers, they should be mounted to the module frame to minimize their temperature rise.

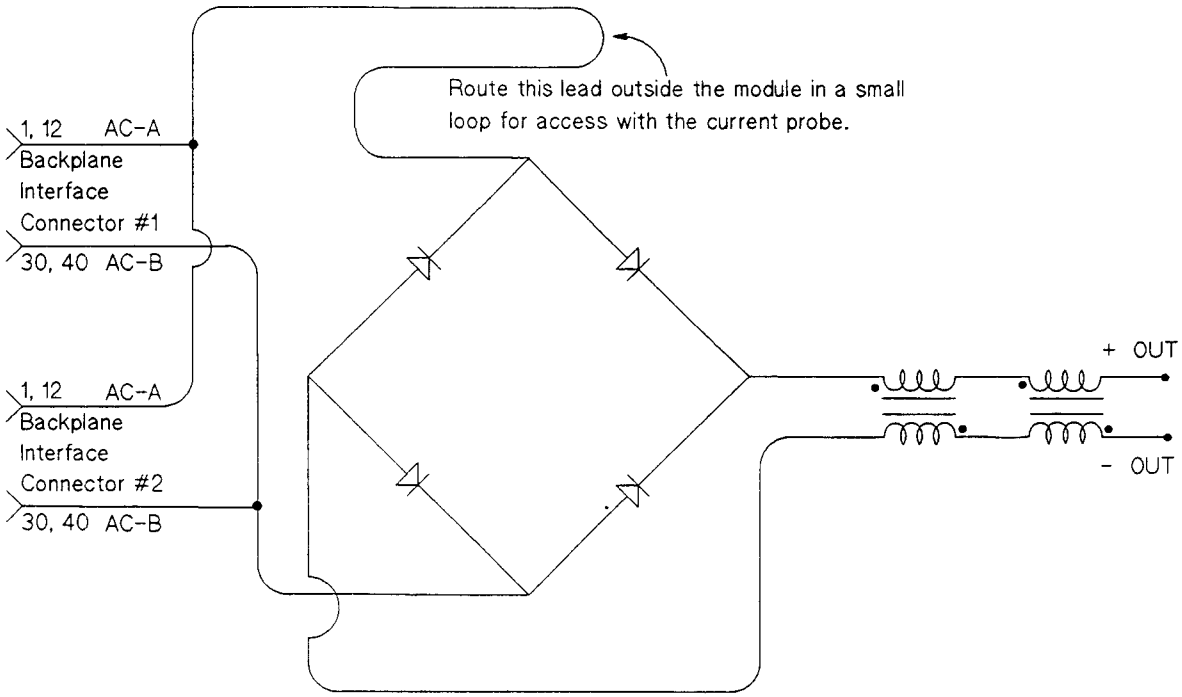


Figure B-17. Nonlinear Load ET

The transformers are wound on Ferroxcube 3622 pot cores, part number 3622PA160-3C8. The part number for a two section bobbin for this core is 3622F2D. Each winding is 14 turns of 17 gauge stranded magnet wire. The module's +Out and -Out terminals should be banana plugs, as they will have to pass several amperes of current.

The individual backplane interface connectors are rated for a maximum load of 100 watts each. Therefore, if a 200 watt mainframe is to be tested, two connectors should be used and wired in parallel. A single connector may be used, but at the risk of damaging the mainframe's connector.

When using this module, it will be necessary to use a current probe to measure the current drawn by the module. For this reason, the wire carrying the module's input current is looped outside the module itself. This provides a convenient place to attach a current probe to the wire.

B.3.1.2.4 Construction Procedure for the Current Injection ET

The current injection ET is used inject a common mode signal into both phases of the 40 kHz power bus. A schematic for the ET is shown in figure B-18.

Because the grounding method used will affect the measurement results, it is important that grounding for this circuit be done in a consistent way. For this reason, the ET should be built into a one slot width module.

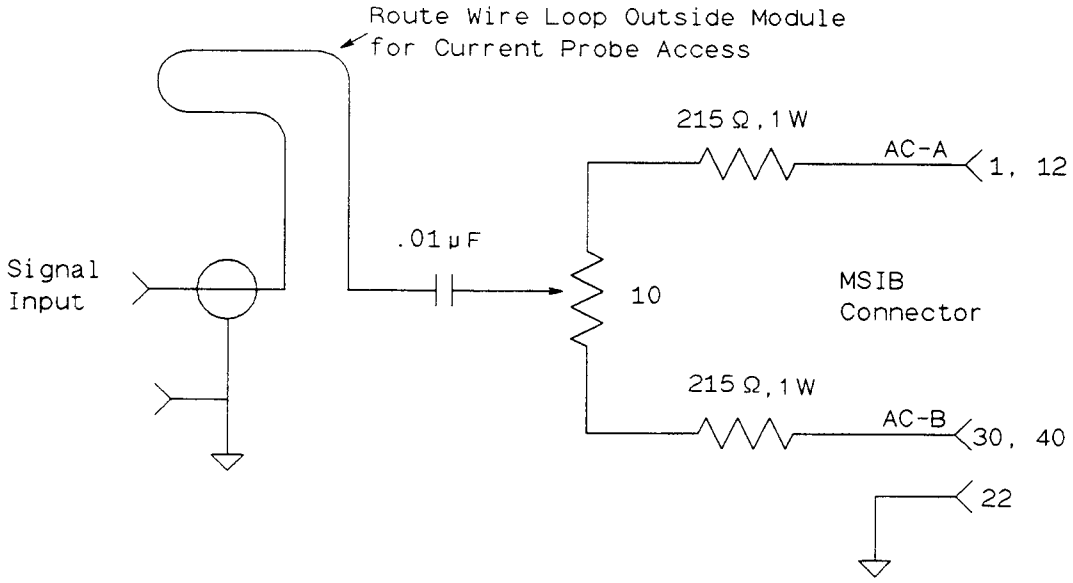


Figure B-18. Current Injection ET

The test using the current injection ET requires that the current into the ET be measured. Because of this, the wire carrying the input signal in the ET is looped outside the module. This provides a convenient place to connect a current probe.

A potentiometer is provided to adjust the balance of the circuit. To perform this adjustment, insert the module into a mainframe. Connect the signal input to a 50 ohm oscilloscope. Adjust the potentiometer until the minimum signal level is displayed on the oscilloscope.

B.3.2 Module Power Bus Conducted Emissions and Susceptibility

B.3.2.1 Module Power Bus Conducted Emissions

This test measures the current drawn from the mainframe by the module under test. To reduce interference between different modules using the bus, the conducted emissions of each module must be tested.

In order to maintain standard grounding, it is important for the module under test to be in a mainframe when the test is performed. The current can be measured by putting the current probe around an appropriate point in the module power supply. It may be convenient to replace the module fuse with a short wire, and to attach the current probe here. Note that there should be no electrical components, such as capacitors or resistors, between the measurement point and the mainframe. If there are, for example, filter capacitors between the measurement location and the mainframe, the measurement will be inaccurate.

B.3.2.1.1 Equipment Needed

- Low Frequency Current Probe: DC-50 MHz Response (e.g. Tektronix A6302),
- High Frequency Current Probe, 50-200 MHz (construction details for this probe are described in section B.3.1.2.3,
- MMS mainframe (e.g., HP 70001A),
- Spectrum analyzer, 100 Hz to 200 MHz (e.g., HP 71100C).

B.3.2.1.2 Test Procedure

There are three distinct specifications for module conducted emissions:

1. Emissions that are harmonics of the 40 kHz load current waveform,
2. Spurious emissions that are not harmonically related to the load current waveform,
3. Modulation sidebands on the 40 kHz load current waveform.

Procedures for tests one and two are described below. The measurement procedure for test three is described in the section B.1.2.1.

The hardware setup for each of these measurements is similar; refer to figure B-19. The module under test is inserted into the mainframe. For measurements below 50 MHz, the low frequency current probe is used to measure current through the leads. The output of the current probe's amplifier is monitored on the spectrum analyzer. For measurements above 50 MHz, a high frequency current probe must be constructed; refer to section B.3.1.2.3 for more information. For these measurements, either the AC-A or AC-B loop is routed through the center of the probe, and the probe's output is monitored directly on the spectrum analyzer. It will be necessary to remove one probe from the loop when the other one is being used, as the extra series impedance caused by the presence of the second probe could affect the measurement results.

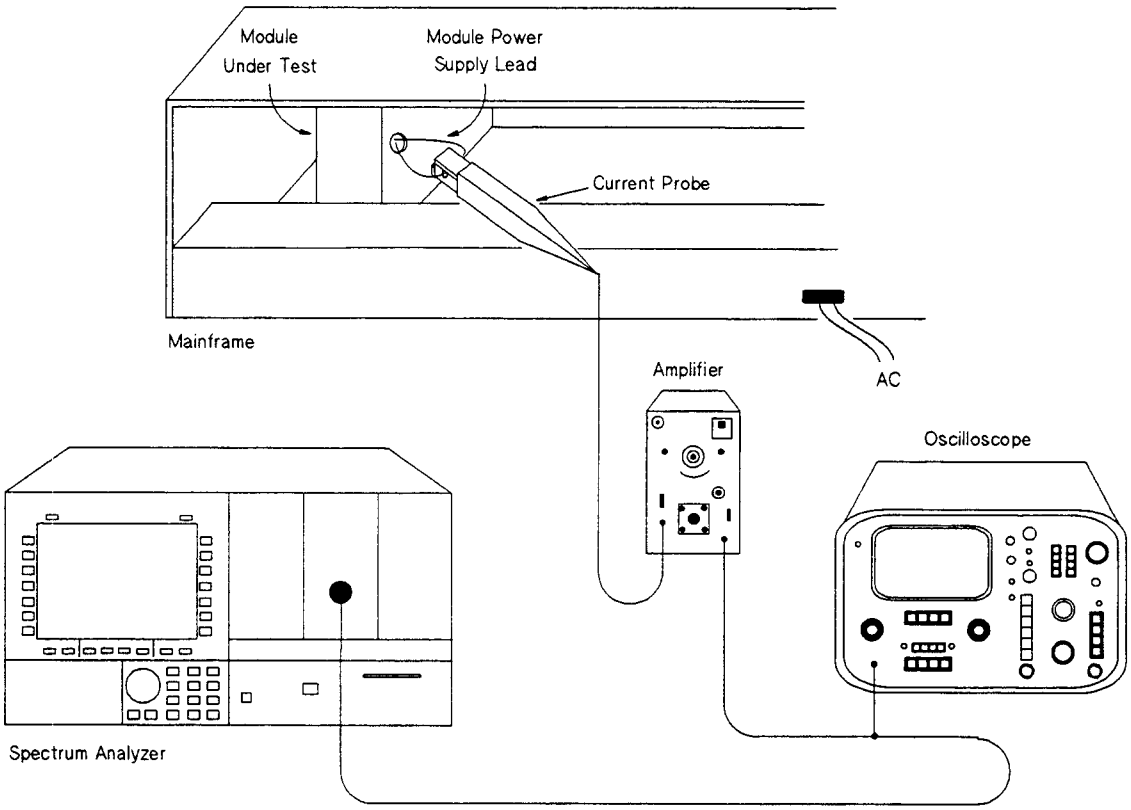


Figure B-19. Module Conducted Emissions Test Setup

When using the low frequency current probe, the output should be monitored on an oscilloscope. This is necessary to prevent clipping in the amplifier. The gain of the amplifier should be adjusted as high as is possible without distorting the waveform shown on the oscilloscope.

40 kHz Harmonics: Limits for 40 kHz harmonically related conducted emissions are shown in figure B-20. The amplitude of a module's harmonics is proportional to its power consumption. Therefore, the specification limits for harmonics levels are set relative to the module's specified power consumption. Because the power supply load presented by the module to the mainframe is balanced, identical results should be obtained when measuring current in AC-A and AC-B. It is therefore only necessary to measure the current in AC-A for this test. For this test, the measurement bandwidth should be at least 5 kHz so that any significant modulation sidebands are included. Otherwise, the measured emissions could be lower than the actual levels.

These limits are specified relative to the maximum allowed 40 kHz current drawn by the module. The approximate amplitude of the 40 kHz component of a module's load current can be calculated from

$$I_{40kHz\,RMS} \approx I_{avg} \times \left.\frac{peak}{avg}\right|_{sine} \times \left.\frac{RMS}{peak}\right|_{sine}$$

$$I_{40kHz\,RMS} \approx \frac{P}{24.3} \times \left(\frac{\pi}{2}\right) \times \left(\frac{1}{\sqrt{2}}\right) \text{ Volts}$$

where P is the specified module power consumption in watts.

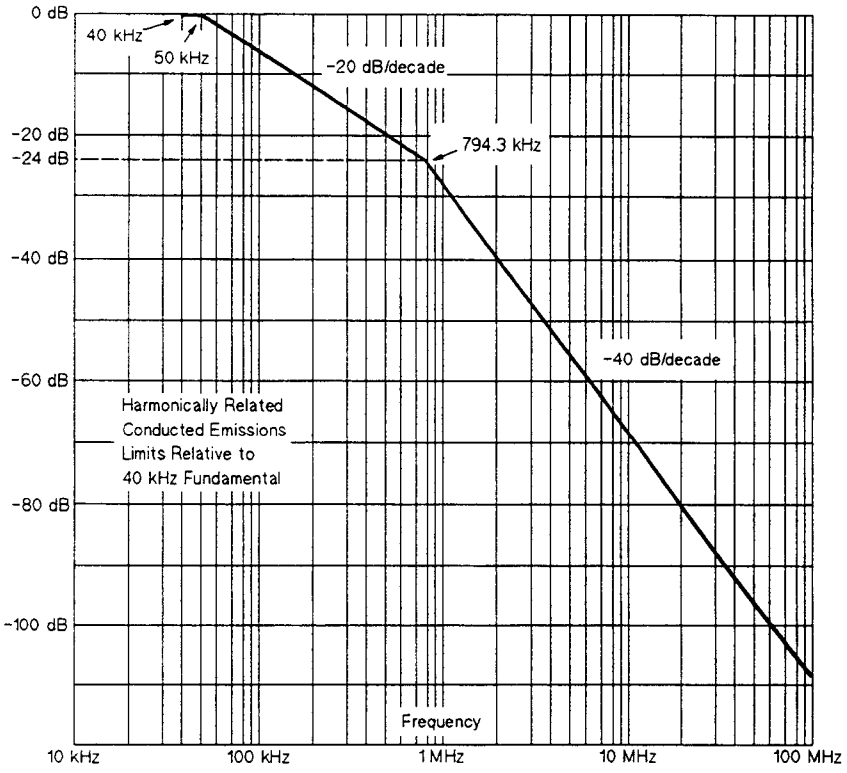


Figure B-20. Module 40 kHz Harmonic Conducted Emissions Limits Relative to 40 kHz Current

Where the limits of figure B-20 fall below the limits of figure B-21, the limits of figure B-20 shall apply.

Non-harmonic Emissions: Limits for power supply non-harmonic spurious emissions are shown in figure B-21. Experience has shown that these emissions are primarily common mode.

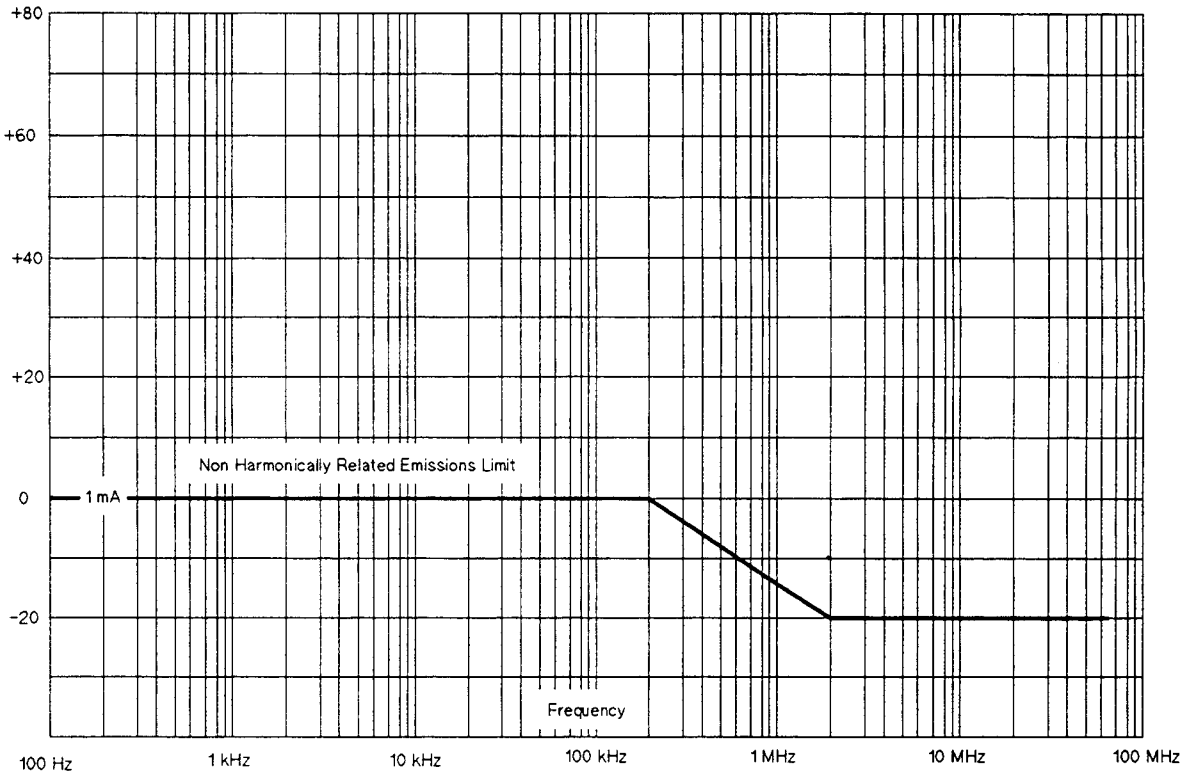


Figure B-21. Module 40 kHz AC Supply Conducted Emissions Limits

For this reason, the test measures only the common mode non-harmonic currents. Common mode currents can be measured by routing the wire loops for both the AC-A and AC-B phases throughout the current probe simultaneously. Be sure that both wires run through the probe in the same direction, or the probe will measure differential mode instead of common mode currents. It may be necessary to temporarily splices smaller gauge wires in series with the current loops so that both will fit within the current probe simultaneously. These should be removed when the test is completed.

B.3.2.1.3 Construction and Calibration of High Frequency Probe

The low frequency probe specified for current measurements has insufficient high frequency response to measure module current emissions over the full frequency range of the specification. It will therefore be necessary to construct another probe to cover the upper portion of the frequency range.

B.3.2.1.3.1 Construction

The high frequency current probe is constructed by winding a transformer on a toroidal core. Seven turns of 32 gauge magnet wire are wound around two small ferrite toroids (Krystinel L21-6K3F-1Q/1). A small 51.1 ohm resistor is soldered in parallel, and the leads are then soldered to an SMB connector (figure B-22). Good high frequency construction techniques should be used, and all leads should be kept as short as possible.

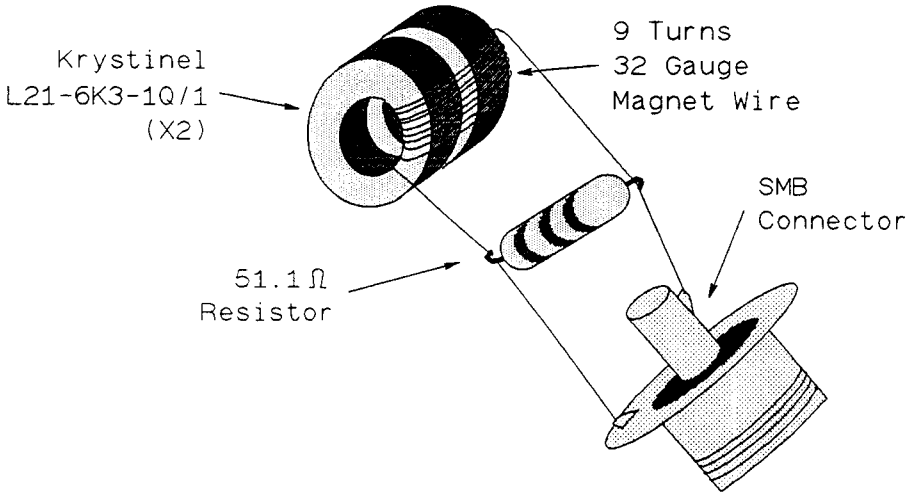


Figure B-22. High Frequency Current Probe

B.3.2.1.3.2 Calibration

To measure current with this probe, a wire carrying the current to be measured is threaded once through the center of the core. The sensitivity of the probe can be measured by connecting the probe to a network analyzer as shown in figure B-23. The network analyzer's output is terminated in a 51.1 ohm resistor. One lead of this resistor is routed through the center of the current probe. The current probe's output is connected to the network analyzer's input. The current through the 51.1 ohm resistor can be calculated from the power delivered to it. A conversion factor for input current to output power can then be calculated for the probe.

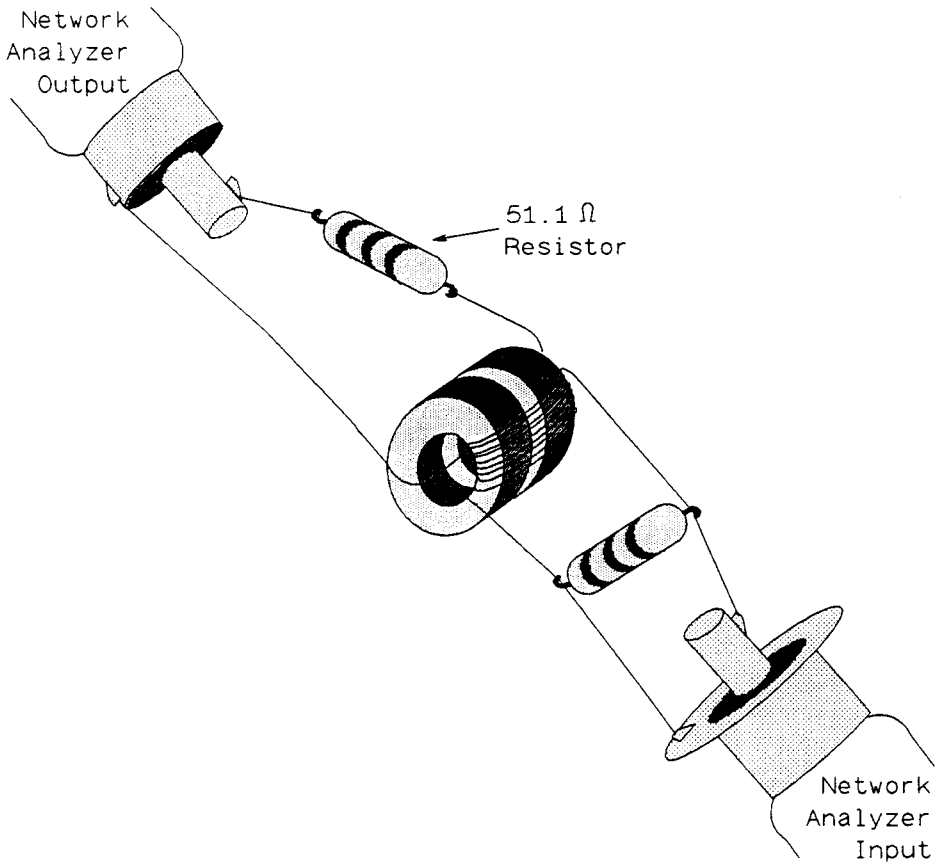


Figure B-23. High Frequency Current Probe Calibration

B.3.2.2 Module Power Bus Conducted Susceptibility

In this test, a voltage is induced on the 40 kHz power supply bus. The module under test is monitored for performance degradation.

Transformers will be wound to induce a voltage into the module power supply leads. It will be necessary to gain access to the module's 40 kHz power supply for this test. It may be convenient to replace the module fuse with a short wire, and to attach the transformers here. Note that there should be no electrical components, such as capacitors or resistors, between the measurement point and the mainframe. If there are, for example, filter capacitors between the measurement location and the mainframe, the measurement will be inaccurate.

B.3.2.2.1 Equipment Needed

- MMS mainframe (e.g., HP 70001A),
- High frequency transformer (described below),
- Low frequency transformer (described below),
- Low frequency spectrum analyzer (e.g., HP 71100C),
- 100 Hz to 200 MHz signal source (e.g., HP 8656),
- 40 kHz notch filter (described below).

B.3.2.2.2 Construction of High and Low Frequency Transformers

Two transformers will be used to inject signals into the power supply bus: a high frequency transformer for the 100 kHz to 200 MHz frequency range and a low frequency transformer for 100 Hz to 100 kHz.

High Frequency Transformer: For the primary, wind 20 turns of 28 gauge magnet wire on a ferrite toroid. Use Fair-Rite Part number 5943000201 for the toroid. Solder a 10 Ω resistor in series with the primary leads, and then solder a bulkhead-mount SMB connector (M/A-Com 5164-5005-09) to the leads. Using the same gauge wire, wind a one-turn secondary on the same core (figure B-24). Solder the leads of this winding to a similar SMB connector. Thread a section of heavy-gauge wire through the center of the core. This wire will carry the module's full load current, so make sure it is heavy enough.

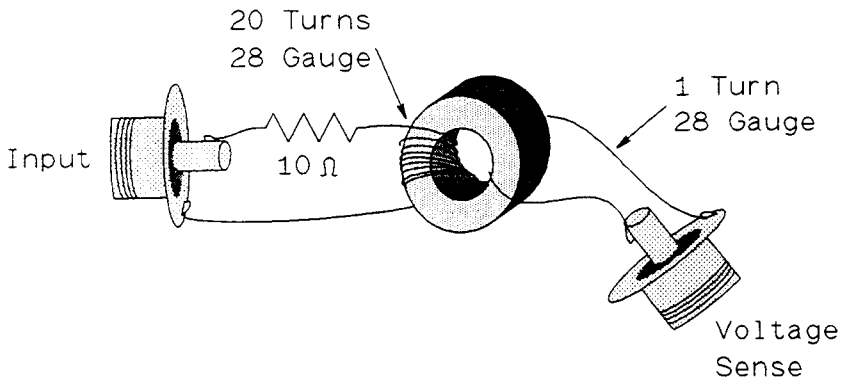


Figure B-24. High Frequency Transformer

In order to contain magnetic fields from the transformer, it will be necessary to mount this entire assembly inside a metal can. Drill two holes for the SMB connectors in an appropriately sized can (Hudson Tool & Die HU-5794-.562-ST can and HU-5794-CA-CRS lid). Also make two small holes to thread the heavy wire through. The transformer assembly should be mounted inside this can. Solder the lid to the can.

It will probably be necessary to build a 40 kHz notch filter to use with this transformer. The purpose of this filter is to protect the signal source used to drive the transformer from the 40 kHz signal. The filter shown in figure B-25 should be sufficient to protect most sources. It should be built in a metal can for shielding.

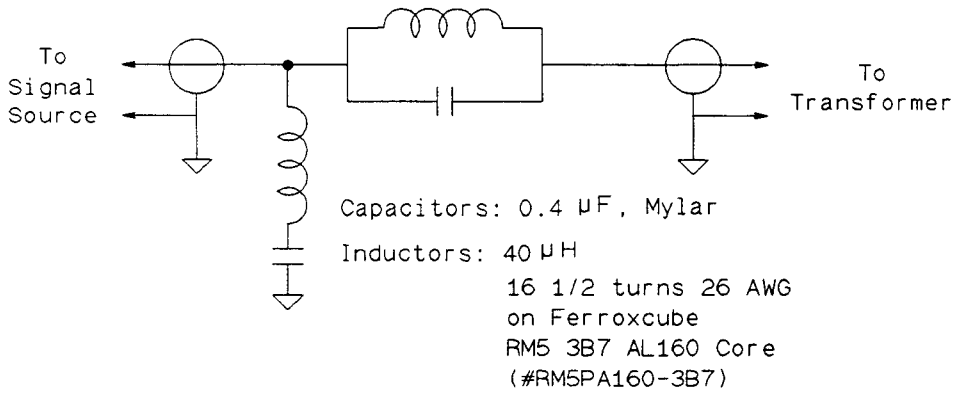


Figure B-25. Low Pass Filter

Low Frequency Transformer: For the primary, wind 300 turns of 28 gauge magnet wire on an RM10 bobbin (TDK BRM-10-7110SD) (figure B-26). Use a TDK H7C1 RM10Z-12 core. Wind two one-turn secondaries with 22 gauge magnet wire. One of these secondaries will be used to monitor the induced secondary voltage. The other will be used to induce a voltage in the power supply. Solder a 1 kΩ resistor in parallel with the primary leads, and then connect a 10 Ω resister in series with an SMB connector to the primary. Solder the leads of one of the secondaries to another SMB connector. This transformer will be used over the frequency range of 100 Hz to 100 kHz. Because of the higher turns ratio for this transformer, a notch filter will probably not be necessary.

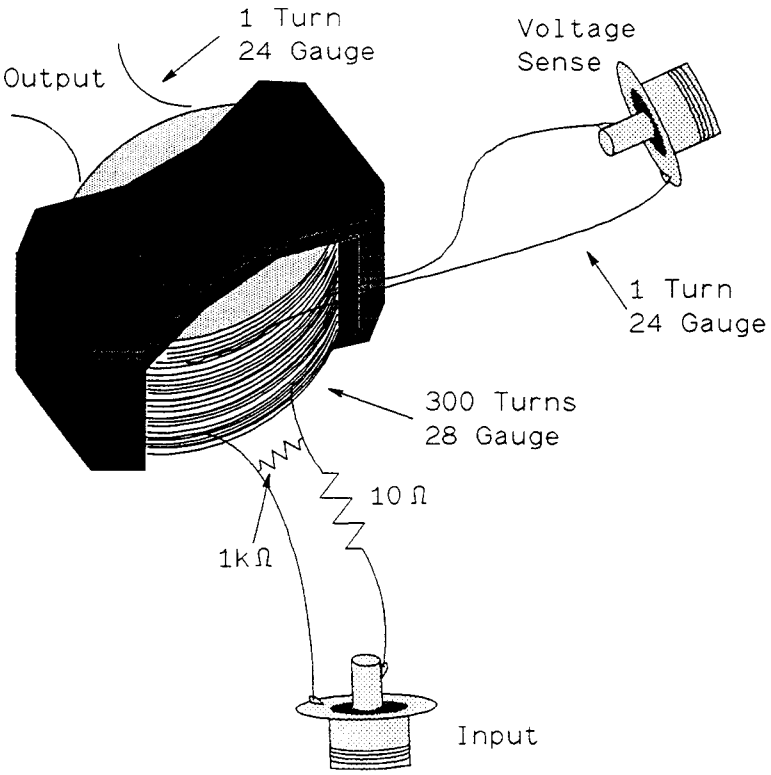


Figure B-26. Low Frequency Transformer

B.3.2.2.3 Test Procedure

This test measures the susceptibility of the module under test to spurious signals induced onto the power supply.

The module under test is inserted into the MMS mainframe. A transformer is inserted in series with either the AC-A or AC-B power supply leads. A signal generator is connected to the transformer to induce a voltage on the power supply, and this voltage is monitored at the transformer's secondary with a spectrum analyzer (figure B-27).

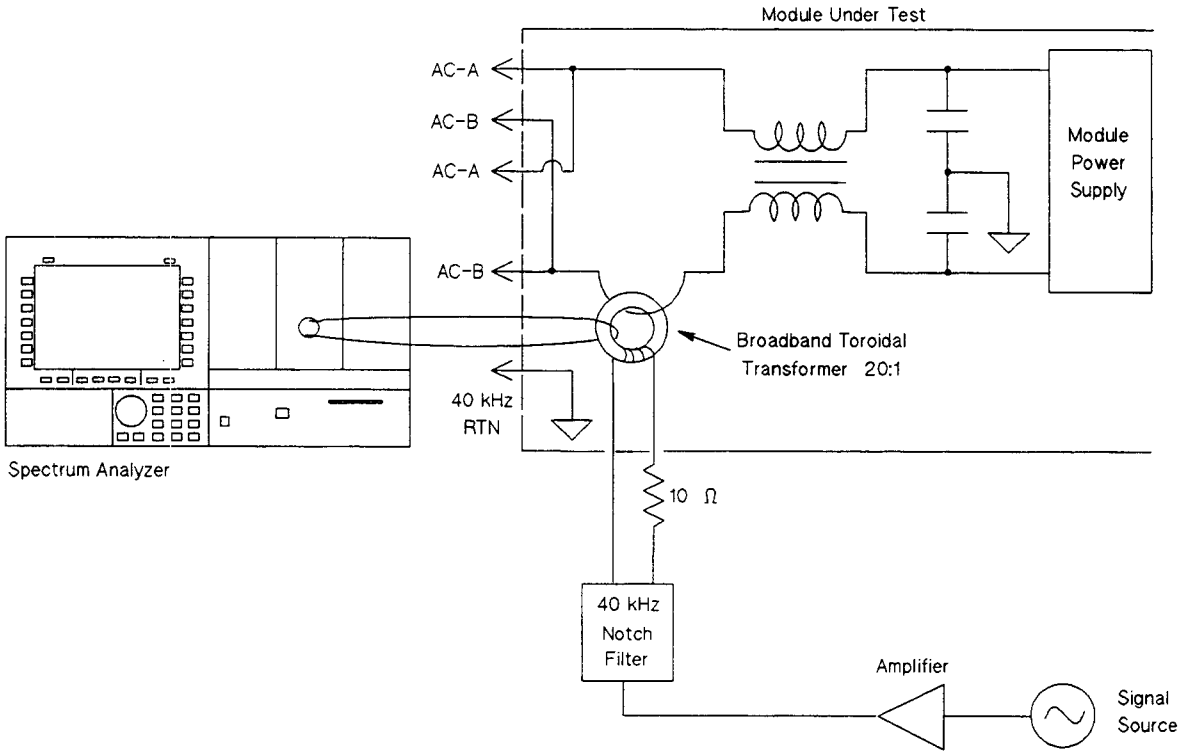


Figure B-27. Conducted Susceptibility Test Setup

Specification limits for this test are shown in figure B-28. The signal generator amplitude should be adjusted until the voltage induced in the secondary is approximately 20 dB above the specified limits. The performance of the module under test is monitored while the frequency of the signal generator is swept over the frequency range of the transformer being used. Where performance degradation is found, adjust the output of the signal generator until performance is degraded to the limits of the module's specifications. Record the signal voltage measured by the spectrum analyzer on the secondary at this point, and compare it to the specification limit. The test should be run twice, once with the transformer inserted in each phase of the power supply.

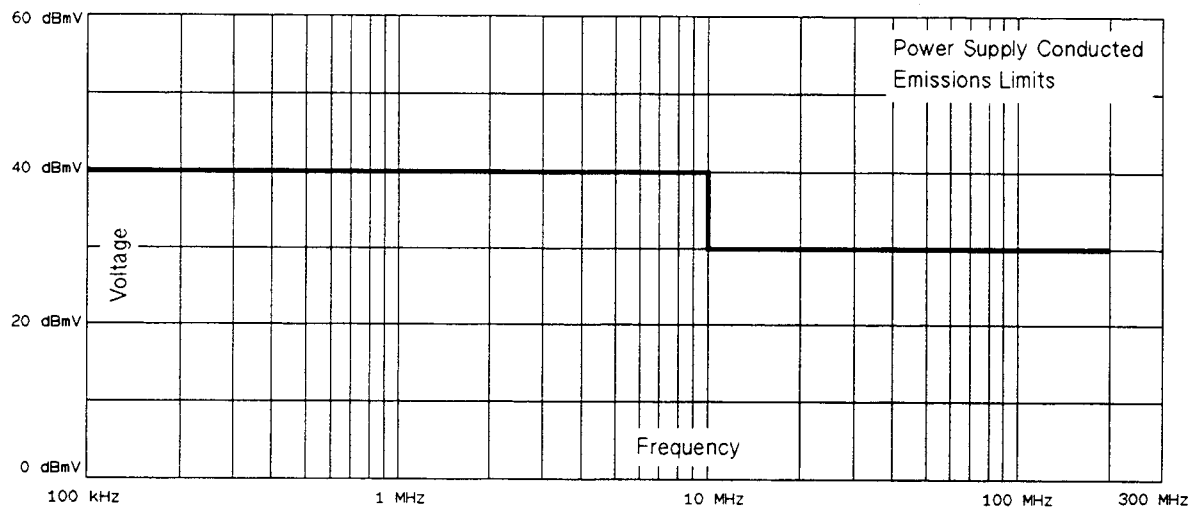


Figure B-28. Module Power Supply Conducted Susceptibility Limit

B.4 Mainframe Microphonic Vibration Test

B.4.1 Equipment Needed

- Dynamic Signal Analyzer (e.g., HP 3582A)
- Charge Amplifier (e.g., Bruel & Kjaer 2635)
- Accelerometer (e.g., Bruel and Kjaer 4393)

B.4.2 Test Procedure

1. Choose an accelerometer appropriate for the dynamic and frequency ranges under test and with the appropriate sensitivity. The accelerometer output should be connected to the spectrum analyzer input through the charge amplifier. Follow manufacturers' recommended instructions for proper installation.
2. Mainframes under test shall be unloaded mainframes.
3. Mainframes under test should be isolated from the external environment to insure that it is not the primary influence on the test results. This can be done, for example, by placing the mainframe on resilient foam and, with the mainframe power off, measuring the "background noise" (see steps 4-5 below for accelerometer placement and spectrum analyzer set-up).
4. Measurements are to be made in all three axes, between all slots, on both the mainframe front and mainframe rear. If desired, the accelerometer may be mounted to a rigid block which in turn is mounted to the mainframe. Manufacturers' recommended instructions for accelerometer mounting should be followed. Figure B-29 shows the suggested block/accelerometer mounting locations.

5. Measurements are to be made over the frequency range of 10Hz to 5kHz, using the following spectrum analyzer set-up:
    1. Bandwidth: 14.5Hz
    2. Measurement Mode: RMS
    3. Passband shape: Flat top
6. Measurements are to be made at all fan operating voltages.
7. Microphonic vibration measured by the procedure outlined in steps 1-6 above must not exceed .010 g's at any test frequency or fan operating voltage, see rule 6.2.4-1.

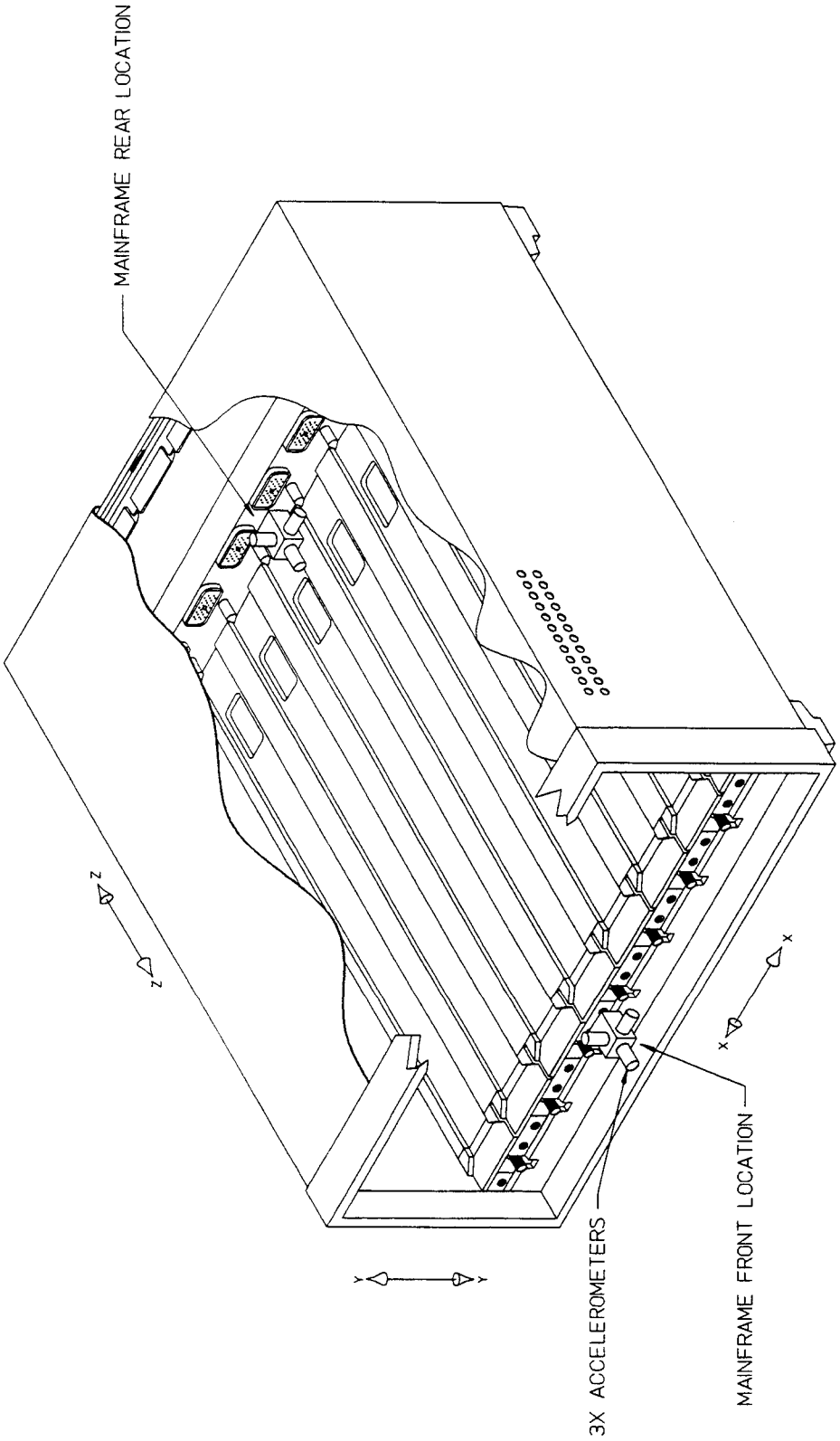


Figure B-29. Microphonic Vibration Accelerometer Locations

B.5 Airflow Tests

B.5.1 Simplified MMS Mainframe Airflow Test Procedure

1. Construct a module pressure drop test chamber as shown in figure B-30.
2. Construct a mainframe airflow test fixture as shown in figure B-31.
3. Use the module pressure drop procedure, see appendix B.5.2, to tune the mainframe airflow test fixture until its operating curve falls at or slightly above the solid line shown in figure 7-2.
4. Turn on mainframe under test and allow the system to reach steady state.
5. Determine airflow by sampling several points in the airflow duct with a hot wire anemometer.
6. Repeat steps 4 and 5 until the "worst slot" is identified.
7. Use the module pressure drop procedure, appendix B.5.2, to tune the mainframe airflow test fixture until its operating curve falls at or slightly above the dotted line shown in figure 7-2.
8. Repeat steps 4 and 5 until the "worst slot" is identified.
9. Check that "worst slot" airflow obtained in step 8 is not a reduction of more than 35% of "worst slot" airflow obtained in step 6.

WARNING: Great care is required to produce accurate results when making airflow measurements. A good understanding of airflow measurement variables is required. For more detailed information on airflow testing, refer to published standards such as ANSI/AMCA 210-85, etc.

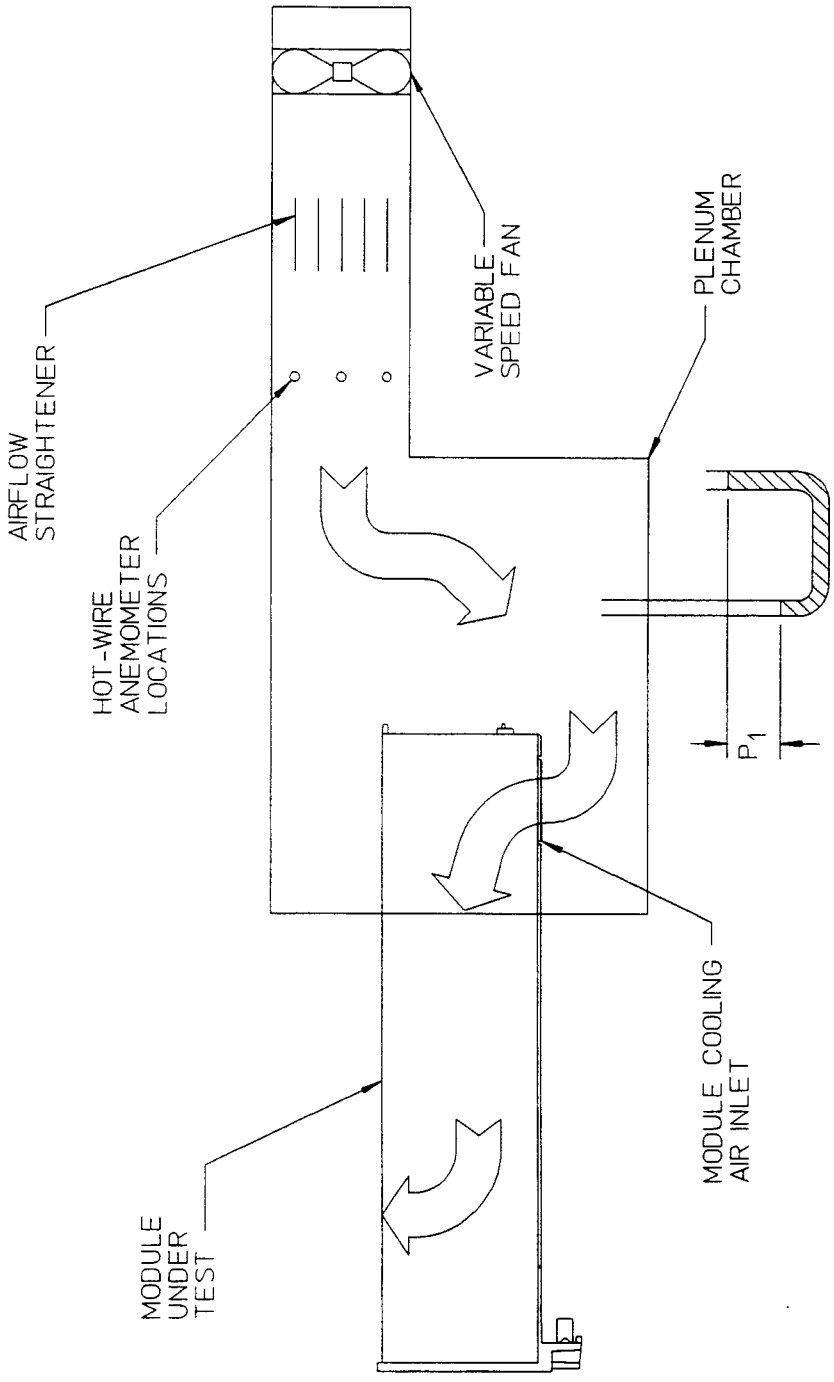


Figure B-30. Simplified Module Pressure Drop Test Chamber

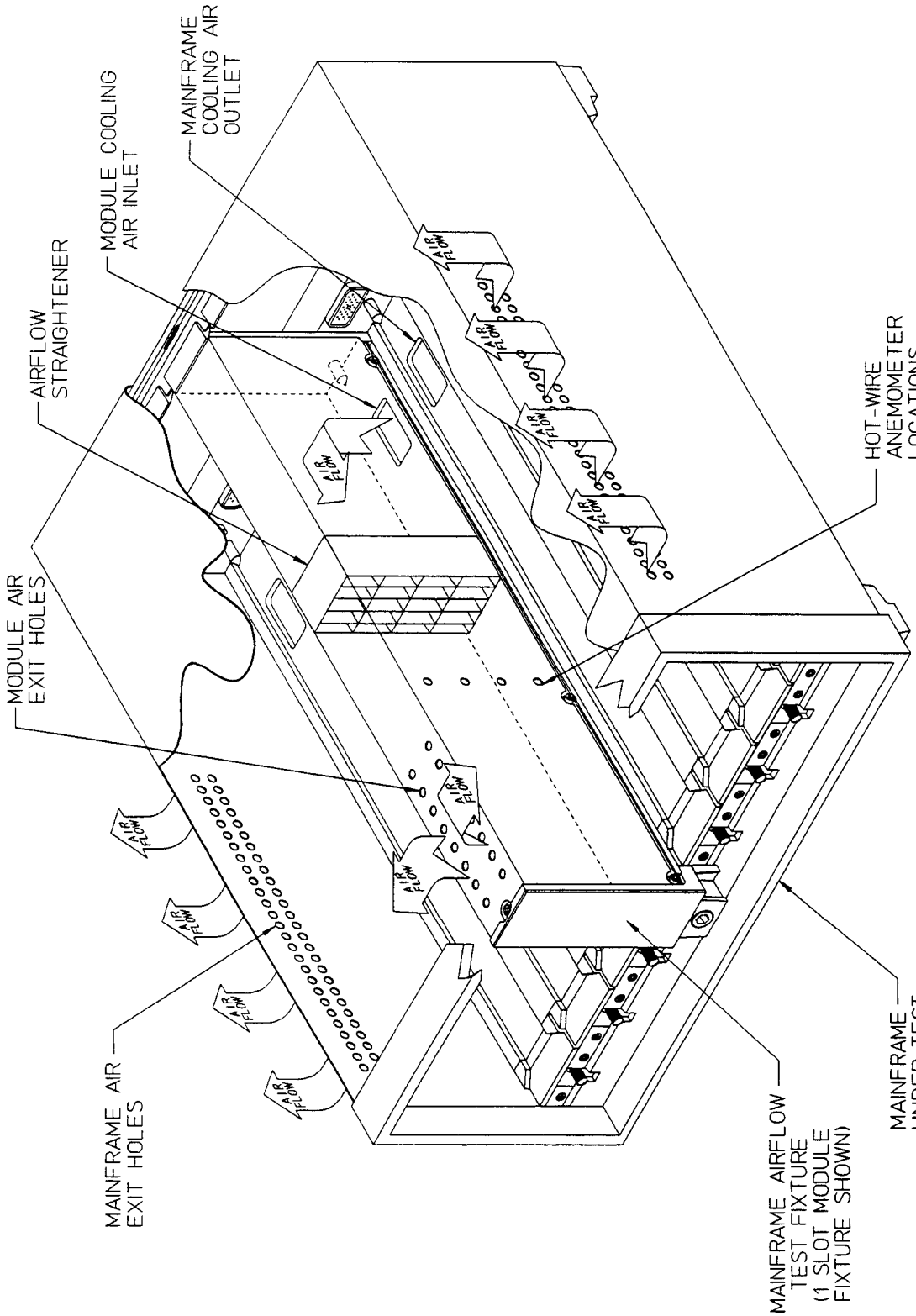

MAINFRAME COOLING AIR OUTLET
MODULE COOLING AIR INLET
AIRFLOW STRAIGHTENER
MODULE AIR EXIT HOLES
HOT-WIRE ANEMOMETER LOCATIONS
MAINFRAME AIR EXIT HOLES
MAINFRAME AIRFLOW TEST FIXTURE (1 SLOT MODULE FIXTURE SHOWN)
MAINFRAME UNDER TEST
AIR FLOW

Figure B-31. Simplified Mainframe Test Setup

B.5.2 Simplified Module Pressure Drop Test Procedure

1. Construct a module pressure drop test chamber as shown in figure B-30.
2. Turn on fan and measure airflow by sampling several points in the duct with a hot wire anemometer.
3. Adjust fan speed until the system reaches a steady state condition at the minimum specified airflow required by the module under test.
4. Measure P1, (equal to plenum chamber pressure minus ambient pressure).
5. Compare operating point of (P1, specified airflow) with figure 7-2.
    1. **IF** the operating point falls on or below the solid curve shown,
    2. **THEN** the tested module will receive the minimum airflow specified on any MMS mainframe it is installed in.
    3. **IF** the operating point falls above the solid curve but below the dotted line shown,
    4. **THEN** careful evaluation is required. The minimum airflow called out on the front of the module should reflect the maximum decrease in airflow allowed by mainframes under these conditions, see rule 7.1-5.
    5. Modules whose operating points fall above the dotted line and require airflow for reliable operation are not recommended.

WARNING: Great care is required to produce accurate results when making airflow measurements. A good understanding of airflow measurement variables is required. For more detailed information on airflow testing, refer to published standards such as ANSI/AMCA 210-85, etc.

C. FABRICATION TOLERANCES

C.1 Scope

This specification establishes tolerances for certain part characteristics which are not toleranced directly on MMS part drawings.

Interpret drawings in accordance with ANSI Y14.5M-1982, *Dimensioning and Tolerancing.*

C.1.1 Final Part Size Considerations

For parts that require finishing such as painting, plating, anodizing, etc., the part dimensions and tolerances shall be before coating. There are several exceptions to this rule:

- Thread designations (M5 x 0.8-6H, 6-32 UNC-2B, etc.) apply to the completed part after any treatment, finishing, or plating. Threads to be coated shall be cut to allow for change in pitch diameter.
- Dimensions and tolerances of heat-treated parts shall apply after treatment.

C.1.2 Hole Diameters

Hole diameters are not controlled by title block tolerances. For information related to machined holes, refer to *Hole Diameters* under the *Machining* section in this chapter. For information related to punched holes, refer to *Punched Hole Size* under the *Sheet Metal* section in this chapter.

C.2 Machining

C.2.1 Hole Diameters

Individual drawing title block tolerances shall not apply to round hole dimensioning. Unless otherwise specified on the part drawing, the hole diameter tolerances in Table C-1 shall be used.

TABLE C-1. Hole Sizes and Tolerances

Hole Size	Tolerances
Thru 1 mm (0.039 in.)	± 0.04 mm (0.0015 in.)
Over 1 mm (0.039 in.) Thru 3.5 mm (0.138 in.)	± 0.05 mm (0.002 in.)
Over 3.5 mm (0.138 in.) Thru 7 mm (0.276 in.)	± 0.08 mm (0.003 in.)
Over 7 mm (0.276 in.) Thru 13 mm (0.512 in.)	± 0.13 mm (0.005 in.)
Over 13 mm (0.512 in.) Thru 19 mm (0.748 in.)	+ 0.18 mm (0.007 in.) - 0.13 mm (0.005 in.)
Over 19 mm (0.748 in.) Thru 25 mm (0.984 in.)	+ 0.23 mm (0.009 in.) - 0.13 mm (0.005 in.)
Over 25 mm (0.984 in.)	+ 0.3 mm (0.012 in.) - 0.13 mm (0.005 in.)

Note: The above tolerances should not be used in tap drill situations because in many cases they are too generous for achieving the requirements of FED-STD-H28/2, ANSI B1.13M or IFI-500.

C.2.1.1 Counterbore/Spotface Diameters

Counterbore and spotfaces should comply with diameter tolerances in Table C-1.

C.2.2 Hole Depths

Depth of hole means depth of the specified diameter. Only the cutting tool point may extend beyond that dimension.

C.2.3 Countersinks

Title block tolerances shall apply to countersink diameters. For information related to sheetmetal tolerances of countersinks, refer to *Countersinks* under the *Sheet Metal* section in this chapter.

C.2.4 Screw Threads

C.2.4.1 Screw Thread Class

Screw thread class shall be:

Metric - (M)
External - Class 6g
Internal - Class 6H

C.2.4.2 Gaging and Verification

Metric thread gaging and verification practices shall conform to:

FED-STD-H28/22, Metric Screw - Thread Gages.

Thread form shall comply with:

Metric-ANSI B1.13m. American National Standard Metric Screw Threads-M Profile, or Industrial Fasteners Institute, IFI-500.

Missing, incomplete, or fractured threads shall not be acceptable.

TABLE C-2. Metric Chamfer-Diameter Limits (millimeters)

Thread Size	External	Internal
M1.6	0.94-1.07	1.74-2.02
M2	1.15-1.40	2.16-2.48
M2.5	1.59-1.84	2.68-3.04
M3	1.89-2.27	3.20-3.60
M3.5	2.28-2.66	3.74-4.22
M4	2.50-3.00	4.28-4.84
M5	3.36-3.86	5.32-5.96
M6	4.10-4.60	6.40-7.20
M8	5.74-6.24	8.50-9.50
M10	7.17-7.93	10.60-11.80
M12	8.84-9.60	12.70-14.10

C.2.5 Chamfers on Threaded Parts

All internal and external threads shall be chamfered to 45° per side (90° included angle) per the diameter limits in Table C-2.

C.2.5.1 Thread Length Dimension

Whether external or internal, the thread length/depth dimension shall be a minimum requirement. Maximum thread length/depth as well as maximum tap drill depth may be left unspecified providing they do not break through or in any way deform another feature of the part. In both cases, title block tolerances do not apply.

C.2.6 Surface Roughness

Machined surface roughness (Ra), as defined in ANSI B46.1, shall not exceed 1.6 micrometers (63 microinches).

Roughness sampling length shall be 0.8 mm (0.030 in.)

C.2.7 Edge and Corner Conditions

C.2.7.1 Burrs

Loose burrs as well as burrs that may result in personal injury shall be removed. Other burrs are allowed, not to exceed 0.1 mm (0.004 in.). Burrs are not allowed to violate part dimension limits of size.

C.2.7.2 Breaks

Edges and outside corners shall be broken, not to exceed 0.5 mm (0.02 in.), measured as shown below.

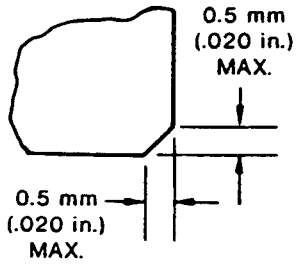
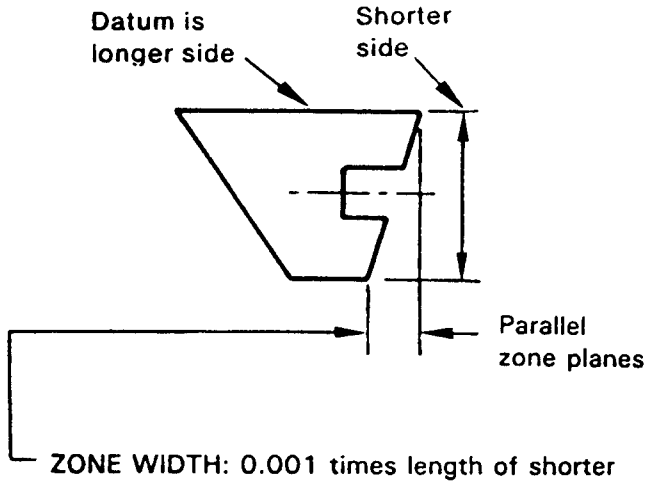


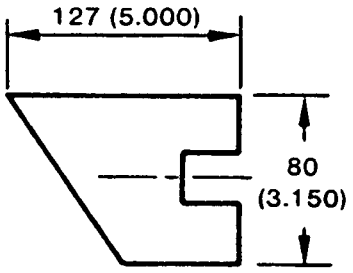
Figure C-1. Edges and Outside Corners Example

C.2.8 Perpendicularity



ZONE WIDTH: 0.001 times length of shorter side, but not to exceed 0.25 mm (.010 in.) MAXIMUM, and not less than 0.03 mm (.001 in.) MINIMUM. Zone is always perpendicular to the datum side.

Example - Zone Width Calculation

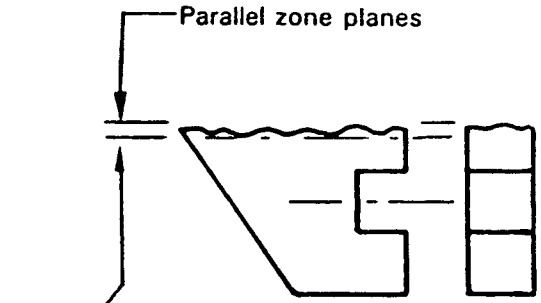


ZONE WIDTH:

0.001 x 80 mm = 0.08 mm
or
0.001 x 3.150 in. = .003 in.

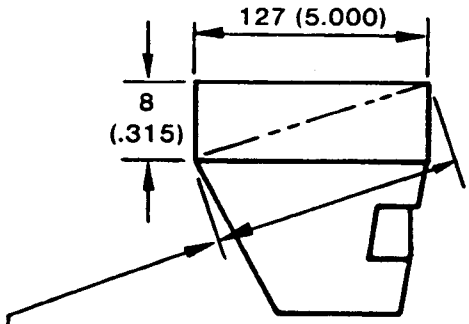
Figure C-2. Perpendicularity Example

C.2.9 Flatness



ZONE WIDTH: 0.001 times longest diagonal, but not to exceed 0.25 mm (.010 in.) MAXIMUM, and not less than 0.03 mm (.001 in.) MINIMUM.

Example - Zone Width Calculation

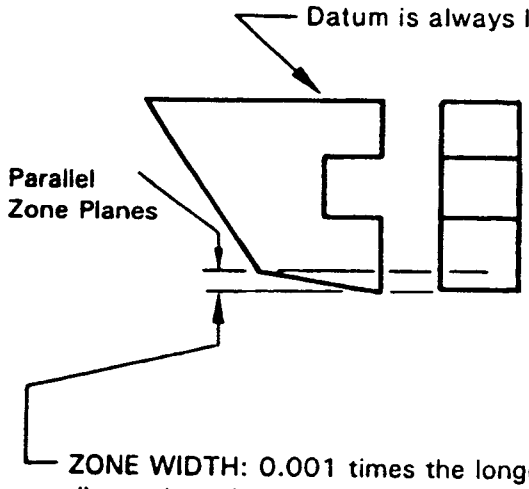


ZONE WIDTH:

Diagonal = 127.25 mm (5.010 in.)
0.001 x 127.25 = 0.13 mm
or
0.001 x 5.010 = .005 in.

Figure C-3. Flatness Example

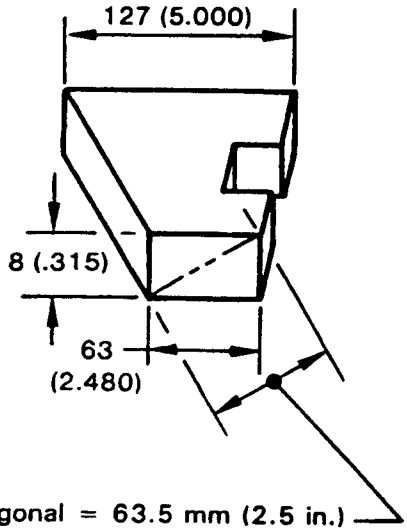
C.2.10 Parallelism



ZONE WIDTH: 0.001 times the longest diagonal on the shorter side, not to exceed 0.25 mm (.010 in.) MAXIMUM, and not less than 0.03 mm (.001 in.) MINIMUM. Zone is always parallel with datum side.

In inspecting for parallelism, only datum side must meet flatness requirements.

Example - Zone Width Calculation

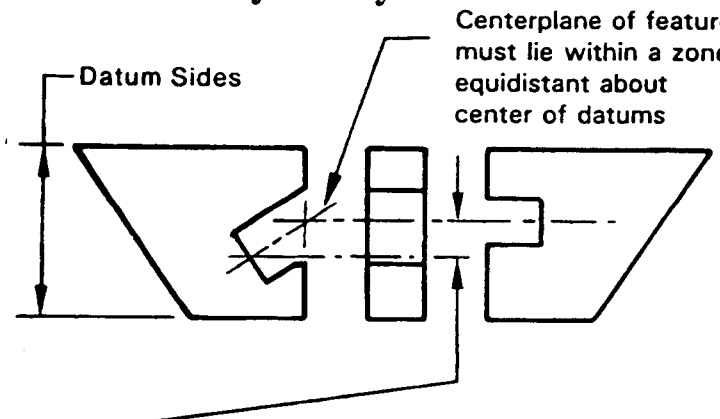


ZONE WIDTH

Diagonal = 63.5 mm (2.5 in.)
0.001 x 63.5 = 0.06 mm,
or
0.001 x 2.500 = .002 in.

Figure C-4. Parallelism Example

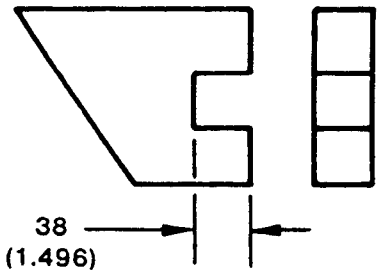
C.2.11 Symmetry



ZONE WIDTH: 0.13 mm (.005 in.) for centerplane features 127 mm (5.000 in.) and shorter; 0.25 mm (.010 in.) for centerplane features longer than 127 mm (5.000 in.).

Zone is always parallel with centerplane of datum sides.

Example - Zone Width Calculation

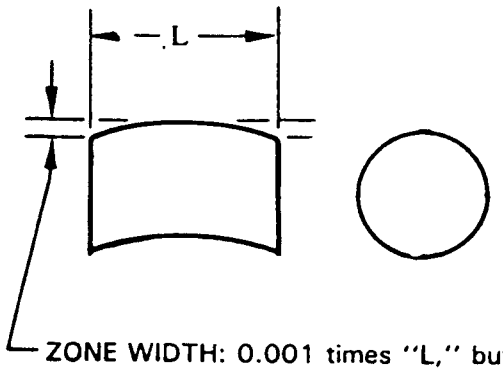


ZONE WIDTH

Since centerplane feature is shorter than 127 mm (5.000 in.), zone width is 0.13 mm or .005 in. If centerplane were for example 190.5 mm (7.500 in.), the zone width would be 0.25 mm or .010 in.

Figure C-5. Symmetry Example

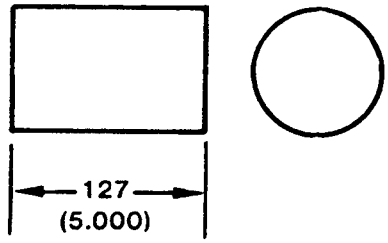
C.2.12 Straightness



ZONE WIDTH: 0.001 times "L," but not less than 0.003 mm (.001 in.).

This applies to cylindrical parts. For other shapes (such as rectangular parts) use Flatness.

Example - Zone Width Calculation

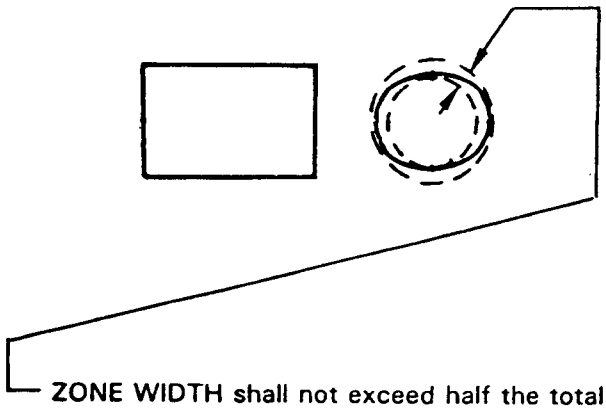


ZONE WIDTH:

0.001 x 127 = 0.13 mm
or
0.001 x 5.000 in. = .005 in.

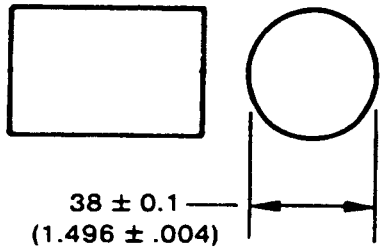
Figure C-6. Straightness Example

C.2.13 Roundness



ZONE WIDTH shall not exceed half the total dimensional tolerance.

Example - Zone Width Calculation



ZONE WIDTH:

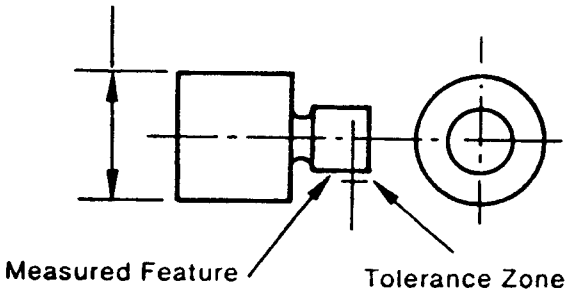
50% of 0.2 mm = 0.1 mm
or
50% of .008 in. = .004 in.

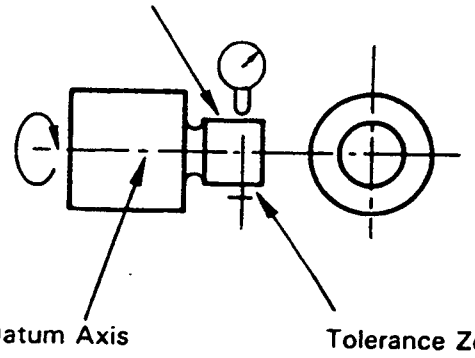
Figure C-7. Roundness Example

C2.14 Circular Roundout

Datum is axis of the longest single feature or largest if features are of equal length.

Any single circular element along measured feature





Tolerance Zone: Any circular element or cross section of measured feature(s) shall not deviate more than 0.13 mm (.005 in.) FIM* relative to datum feature.

Example:

Maximum FIM = 0.13 mm (.005 in.)

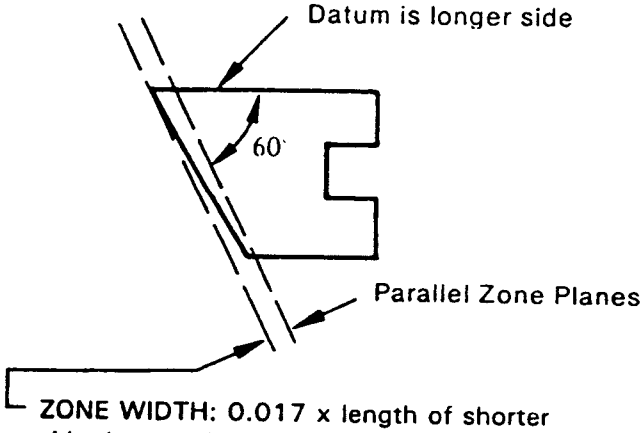
Note: All diameters must comply

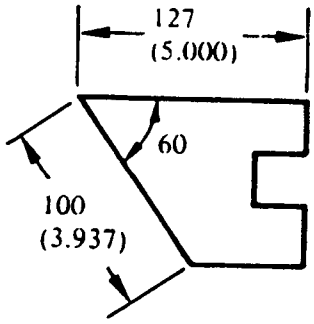
*FIM = Full Indicator Movement Per Y14 1.3.20

Figure C-8. Circular Roundout Example

C2.15 Angularity

Example Zone Width Calculation





ZONE WIDTH: 0.017 x length of shorter side, but not less than 0.03 mm (.001 in.). This tolerance zone is established by contact of the outermost of the two zone planes with the extremities of the angular surface and with the other zone plane placed parallel and inward to the part. The entire surface must fall within this tolerance zone.

ZONE WIDTH:

0.017 x 100 mm = 1.7 mm,
or
0.017 x 3.937 in. = .067 in.

Figure C-9. Angularity Example

C.3 Sheet Metal

C.3.1 Shearing Squareness

Maximum allowable deviation from square (90°), designated or implied, is 0.002 mm per mm length or 0.002 inch per inch length, given the following constraints:

1. Length and deviation measurements must be measured along the shorter of the adjacent sides being checked.
2. For lengths longer that 150 mm or 6 inches, maximum allowable deviation from square shall be 0.3 mm (0.012 in.).
3. For lengths shorter than 50 mm or 2 inches, deviation up to 0.1 mm (0.004 in.) are allowed.

Shear edge break shall not be considered in this measurement.

C.3.2 Sheared Angles

No deviation from designated angle exceeding ± 1.5°. Shear edge break is not to be considered in this measurement.

C.3.3 Shear Type Burrs

Shear type burrs created by punching, nibbling, notching, blanking, and shearing shall not exceed 0.1 mm (0.004 in.) of protrusion beyond the part surface or into an opening. Loose burrs as well as burrs that may result in personal injury shall be removed.

Surfaces that are to be totally burr free must be specified.

C.3.4 Notch Marks

Notch marks along multi-punched holes, openings, or edges shall not exceed 0.15 mm (0.006 in.), nor violate limits of feature size.

C.3.5 Flatness

No deviation from true flatness exceeding 0.005 mm per mm length or 0.005 inch per inch length, with a maximum of 5 mm (0.20 inch) regardless of length (measured along longest possible dimension, e.g., diagonally across part).

Designer's Note: If this deviation from flatness allowance becomes unacceptable or too generous, an overriding flatness tolerance may be applied to the part drawing.

C.3.6 Folds

No deviation exceeding ± 1.5° in all cases.

C.3.6.1 Multiple Folds

Any two adjacent folds (regardless of fold angle) shall be parallel or perpendicular to each other within 0.5 mm (0.020 in.) along the length of the folds.

C.3.7 Offsets

Designated or implied parallelism between the primary surface and the offset surface shall be within ± 1.5° in all cases.

C.3.8 Measurement of Folds and Offsets

All edge-to-fold, fold-to-fold, and offset height dimensions are to be measured at the tangent points of the radii regardless of the location of the dimension and extension lines.

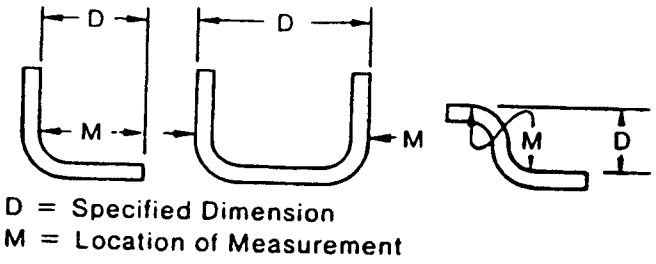


Figure C-10. Sheet Metal Fold Example

C.3.9 Punched Hole Size

C.3.9.1 Single-Hit Holes

Title block tolerances shall not apply to individual punched holes produced by a single hit.

A tolerance of ± 0.08 mm (0.003 in.) unless otherwise noted shall apply to round hole sizes and shaped hole sizes that are produced by a single hit. Shear edge break shall not be considered in this measurement.

C.3.9.2 Multi-Hit Holes

Title block or specified tolerances shall apply to individual holes or openings that are produced by more than one hit. Shear edge break shall not be considered in this measurement.

C.3.10 Countersinks

Any countersink, whether produced by a cutting tool or dimpling die shall be allowed a deviation of ± 0.25 mm (± 0.010 in.) from specified outside diameter.

C.3.10.1 Surface Condition

In the absence of a part drawing notation, all sheet metal parts shall receive mechanical surface treatment on both sides, such as, course sand, circular sand, a tumbled or vibratory finish, but not to the exclusion of other processes. Final appearance shall be uniform. Surface roughness value (Ra) shall be between 0.4 micrometer (16 microinch) and 2.3 micrometer (90 microinch).

C.4 Standards for Other Processes

Tolerances for part processes not included in this Std./Spec. may be contained in industry standards as cited below and shall be used for acceptance or rejection in the absence of tolerances specified directly on the part drawing.

C.4.1 Aluminum Die Casting

Product guidelines for die casting, Sections NADCA E1-65 Metric through NADCA E18-64T Metric. North American Die Casting Association, 2000 N. Fifth Ave., River Grove, IL 60171-1992 (formerly American Die Casting Institute (ADCI)).

C.4.2 Plastic Molding

Standards and Practices of Plastics Molded Parts Buyers Guide, (1978 or later issue). The Society of Plastics Industry, Inc., 1275 K Street N.W., Washington, D.C. 20005.

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D. APPLICATION FOR MMS MANUFACTURER'S IDENTIFICATION

Identification of the manufacturer of a logical module is a required response to an MSIB command. The identification string must be registered with the MMS Consortium. There is no charge for registering an identification string. One identification string per company is expected. If more than one identification string is necessary, please provide an explanation with this application.

_____
Date

_____
Company Name

_____
Company Representative Title

_____

_____

_____
Address

Requested Identification String:

_____
Manufacturer ID String

Any number of uppercase or lowercase characters, spaces, or punctuation represented by the ASCII character set may be used.

Notification of acceptance of the Requested Identification String will be provided to the company representative listed on this form.

Mail to the MMS Consortium:

MMS Consortium
c/o Tom Hoppin, Secretary
Hewlett-Packard Company
1212 Valley House Drive
Rohnert Park, Ca. 94928

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